Reg. No. | | | | | | | | | | | | |

Question Paper Code : 57234

B.E/B.Tech. DEGREE EXAMINATION, MAY/JUNE 2016

Second Semester

Computer Science and Engineering

CS 6201 – DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulations 2013)

Time : Three Hours **Maximum : 100 Marks**

Answer ALL questions.

PART – A (10 × 2 = 20 Marks)

1. Find the Octal equivalent of the hexadecimal number DC.BA.
2. What is meant by multilevel gates network ?
3. Define Combinational circuits.
4. Design the combinational circuit with 3 inputs and 1 output. The output is 1 when the binary value of the inputs is less than 3. The output is 0 otherwise.
5. State the excitation table of JK-Flip Flop.
6. A seven bit Hamming code is received as 1111110. What is the correct code ?
7. What is the minimum number of flip flops needed to build a counter of modulus 8 ?
8. What is lockout ? How it is avoided ?
9. Define the critical rate and non critical rate.
10. Draw the wave forms showing static 1 hazard ?

PART – B (5 × 16 = 80 Marks)

11. (a) Reduce the expression using Quine McCluskey method.

$F(x_1, x_2, x_3, x_4, x_5) = \sum m(0, 2, 4, 5, 6, 7, 8, 10, 14, 17, 18, 21, 29, 31) + \sum d(11, 20, 22)$ **(16)**

OR

(b) Determine the MSP form of the Switching function F (a, b, c, d) = _ (0, 2, 4, 6, 8) + _d(10, 11, 12, 13, 14, 15). **(16)**

12. (a) Design a full adder with inputs *x*, y, z and two outputs S and C. The circuits performs *x* + y + z, z is the input carry, C is the output carry and S is the Sum. **(16)**

OR

(b) Design a logic circuit that accepts a 4-bit Grey code and converts it into 4-bit binary code. **(16)**

13. (a) Implement the following Boolean function with a 4 × 1 multiplexer and external gates. Connect inputs A and B to the selection lines. The input requirements for the four data lines will be a function of variables C and D these values are obtained by expressing F as a function of C and D for each of the four cases when AB = 00, 01, 10 and 11. These functions may have to be implemented with external gates. F(A, B, C, D) = ∑ (1, 2, 5, 7, 8, 10, 11, 13, 15). **(16)**

OR

(b) Draw a neat sketch showing implementation of Z_1 = ab'd'e + a'b'c' e + bc + de, Z_2 = a'c'e, Z_3 = bc + de +c'd'e + bd and Z_4 = a'c'e + ce using a 5*8*4 PLA. **(16)**

14. (a) Design a binary counter using T flip-flops to count in the following sequences :

(i) 000, 001, 010, 011, 100, 101, 111, 000

(ii) 000, 100, 111, 010, 011, 000 **(16)**

OR

(b) Design a modulo 5 synchronous counter using JK Flip Flop and implement it. Construct its timing diagram. **(16)**

15. (a) Design an asynchronous sequential circuit with 2 inputs X and Y and with one output Z Wherever Y is 1, input X is transferred to Z. When Y is 0; the output does not change for any change in X. Use SR latch for implementation of the circuit. **(16)**

OR

(b) Discuss in detail the procedure for reducing the flow table with an example. **(16)**