## QUESTION PAPER CODE: 10291

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2012.

THIRD SEMESTER

ELECTRONICS AND COMMUNICATION ENGINEERING

## EC 2205/147304--ELECTRONIC CIRCUITS-I

(REGULATION 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A--(10 × 2 = 20 marks)

1. Define stability factor.
2. What are the different methods of biasing JFET?
3. Define Miller's theorem.
4. Give the voltage gain for CE configuration including source resistance.
5. If the rise time of a BJT is 40 nano seconds, what is the bandwidth tht can be obtained using this BJT?
6. Why is it not possible to use the h-parameters at high frequencies?
7. Draw a quasi complementary symmetry power amplifier?
8. What is the advantage of using the output transformer for a class A amplifier?
9. Prove that the ripple factor of a half wave rectifier is 1.21 and that of a full wave rectifier is 0.482.
10. Write the expression of ripple factor for capacitor input filter.

PART B--(5 × 16 = 80 marks)

11. (a) Draw a voltage divider bias BJT network. Derive expressions for $I_{CQ}$ and $V_{CEQ}$ and describe the method of drawing the dc load line on the output characteristics of transistor. (16)

(or)

11. (b) Comment on fixed biasing in BJT and FET. Explain the procedure for locating suitable operating point on the characteristic curves. (16)

12. (a) (i) Explain with circuit diagram the boot strapped Darlington emitter follower. (8)

12. (a) (ii) A CC amplifier is fed with voltage source $V_S$ of internal resistance $R_S = 800\ ohm$. The load resistance $R_L = 1600\ ohm$. The CE hybrid parameters are $h_{ie} = 1000\ ohm$; $h_{re} = 2.2 \times 10 - 4$; $h_{fe} = 55$; $h_{oe} = 23\ \mu\ A/v$. Compute voltage gain, current gain, input resistance, output resistance using approximate analysis. (8)

(or)

12. (b) Draw the small signal hybrid model of CE amplifier and derive the expression for its $A_I$, $A_V$, $R_i$ and $R_o$. (16)

13. (a) (i) Draw the high frequency hybrid $\pi$ model for a transistor in the CE configuration and explain the significance of each component. (12)

13. (a) (ii) Define alpha cut off frequency. (4)

(or)

13. (b) (i) Define the frequency response of multistage amplifier and derive its upper and lower cut-off frequencies. (8)

13. (b) (ii) How does Rise and Sag time related to cut-off frequencies? Justify. (8)

14. (a) (i) Draw a neat circuit diagram of push-pull class-B amplifier. Explain its working. (8)

14. (a) (ii) Draw the schematic of MOSFET power amplifier. Explain its operation and characteristics. (8)

(or)

14. (b) (i) Compare class A, class B and class C power amplifier performance and efficiency. **(10)**

14. (b) (ii) Give the design procedure for heat sinks. **(6)**

15. (a) A full wave rectifier circuit is fed from a transformer having a centre tapped secondary winding. The rms voltage from either end of secondary to centre tap is 20V. If the diode forward resistance is 3 ohm and that of the half secondary is 50 ohm, for a load of 1K ohm, calculate

(i) Power delivered to load,

(ii) % regulation at full load,

(iii) Efficiency at full load and

(iv) TUF of secondary. **(16)**

**(or)**

15. (b) (i) Draw the block diagram of switched mode power supplyand explain the operation. **(12)**

15. (b) (ii) Derive the ripple factor for L-C filters. **(4)**