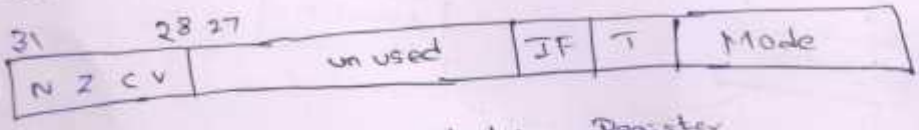
Unit - 4

Introduction to micro processor

1. Explain in brief about ARM Programmer's model:

A Processor instruction set define the operation that the Programmer to change the state of system. Each instruction can be view as performs a defined transformed to state before instruction is executed



The current Program status Register

N: negative, the last ALU operation which change flags produced negative result

Z: zero:- the last ALU operation which change the flag produce a result zero

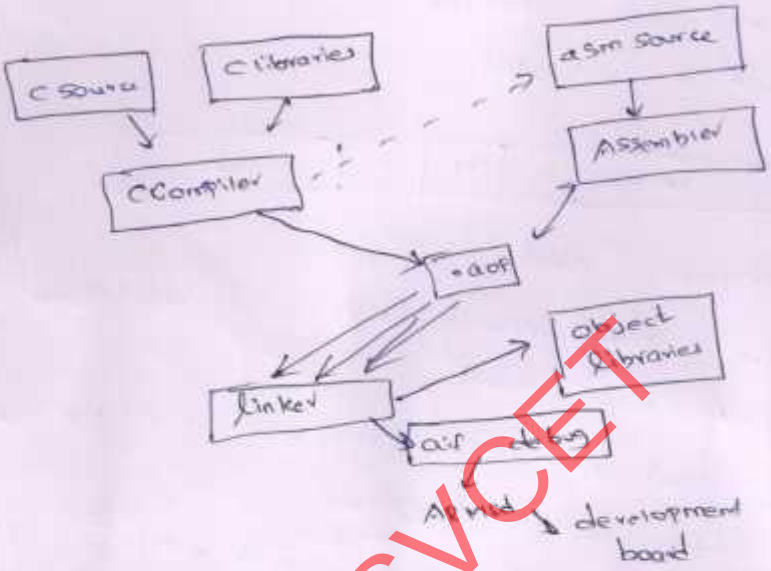
C: Carry:- the last ALU operation which change the flag generated a carry out, either as a result of an arithmetic operation

The memory System:-

In addition the processor register state an RM System state. This shows a small area of memory where each byte location.

2. Explain in detail about ARM development Tools:

Software development for Arm is support by coherent range of tools develop by ARM Limited & there also many third party & public domain tools avail



C or assembler source Files are Compiled or assembled in to ARM object format.

ARM C Compiler:-

ARM C Compiler is Compliant with ANSI standard for C and is support by appropriate library of standard function.

* ARM Assembler
* The Linker

3) Describe the principal Features of ARM Architecture

Certain Features of ARM architecture are

- Large set of registers all which can be used for most purposes
- a load store architecture
- 3 address instruction (two source operand registers & the result register are all independently specified)
- Conditional execution of every instruction
- inclusion of very powerful load
- ability to perform a general shift operation
- open instruction set extension through the Coprocessor instruction set
- very dense 16 bit compressed representation of instruction set in the thumb architecture

4) Explain in brief about Cache design.

The choice of organization for a cache requires the consideration of several Features as discussed

Performance

Cache form

no cache 1

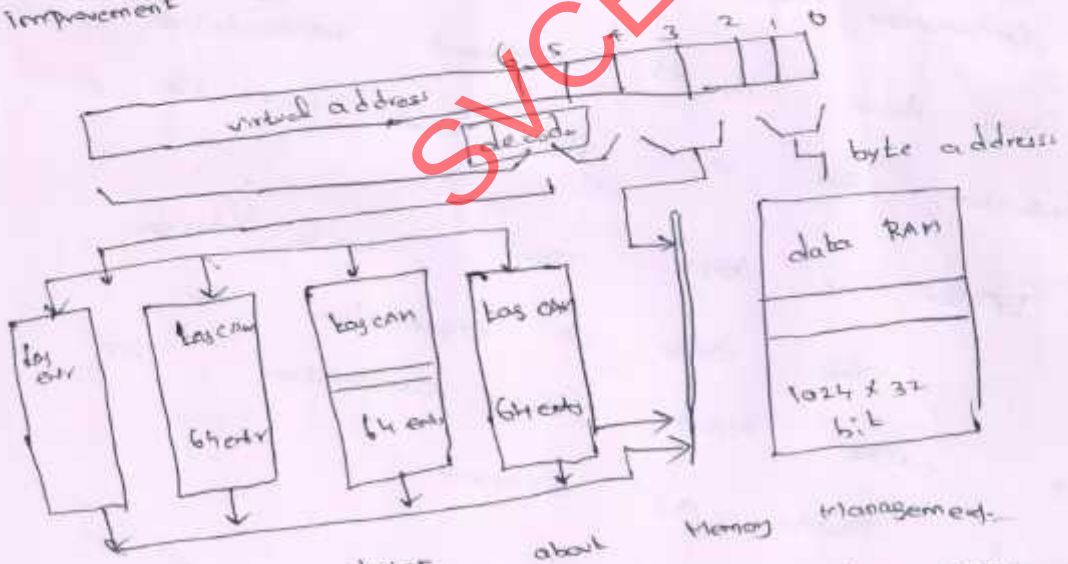
Instruction - any cache 1.95

Instruction & data 2.5

Data any cache 1.13

The simplest cache organization direct mapped cache. but even a size of 16 k bytes the cache is significantly worse 'perfect case' Going to other extreme a fully associate cache performs significantly better at smaller size

the performance of the system for all associatives from fully associative down to direct mapped Although the biggest performance increase is in going from direct mapped to dual-set associate. there are noticable improvement all the way up to 64 way associativity.



5) Explain in brief about Memory management.

Modern Computer System has many program active at same time

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A virtual cache has the many start advantage that the cache access immediately the processor produce an address

A physical cache avoid the synonym Problem since physical memory address are associated with unique data items.

A physical cache arrangement that neatly avoid the sequential access cost exploits the fact that paging MMU only affect the high order address bits. while the cache is accessed.

In Practise both virtual & physical cache are in commercial use the former relying on software convention to contain synonym problem

6 How big would a TLB have to be contain translations For all physical pages?

With 4k byte page, 1 Mbyte memory contain 256 page to TLB needs 256 entries the TLB need no longer be an automatic cache since TLB miss means that page is absent.

Arithmetic operation

ADD r0 r1 r2 ; r0 = r1 + r2
ADC r0 r1 r2 ; r0 = r1 + r2 + C
SUB r0 r1 r2 ; r0 = r1 - r2
SBC r0 r1 r2 ; r0 = r1 - r2 + C - 1
RSB r0 r1 r2 ; r0 = r2 - r1
RSC r0, r1 r2 ; r0 = r2 - r1 + C - 1

AND r0, r1 , r2 ; r0 = r1 & r2
r0 r1 , r2 ; r0 = r1 or r2
FOR r0 r1 r2 ; r0 = r1 x or r2
BIC r0 r1 r2 ; r0 = r1 & not r2

MOV : r0 r2 ; r0 = r2
MVN : r0, r2 ; r0 = not r2.

CMP CMN : r1 r2 : Set cc on r1 - r2
TSTTEQ : r1 r2 : Set cc on r1 + r2

Immediate operands:

Instead of adding two registers we simply wish to add a constant to

register
ADD r3 r3 ; r3 = r3 + 1
AND r8 r7 ; r8 = r8 & fd ; r7(7,0).

16. With neat diagram explain case study in detail how 8051 microcontroller can be interfaced with Liquid Cyrstal Display. (Jan. '15)

17. Explain the case study how the gate signals (assume the switch is SCR or MOSFET) to half bridge single phase converter are generated.

18. Draw and discuss a case study scheme for microcontroller based multichannel data acquisition system.

19. (i) Explain the step mode operation of stepper motors with a control strategy.

(ii) Draw and explain the case study of PWM generation using a PIC Microcontroller.

20. Discuss the case study how PIC microcontroller can control motors. Provide the basic circuitry for doing so.

UNIT–IV

PART-A

1. **What are the basic operating modes of ARM?**

Ans: a) User
b) FIQ
c) IRQ
d) Supervisor
e) Abort
f) Undef
g) System

2. **What is ARM?**

Ans: ARM is short for Advanced Risk Machine Funded in 1990, owned by Acorn, Apple and VLSI. ARM is one of the most licensed company, used especially in portable devices due to low power consumption and reasonable performance (MIPS/Watt).

3. **Write the features of ARM.**

Ans: (1) Architecture simplicity
(2) Very small implementations
(3) Very low power consumption.

4. **Differentiate between User Mode and Exceptions Mode.**

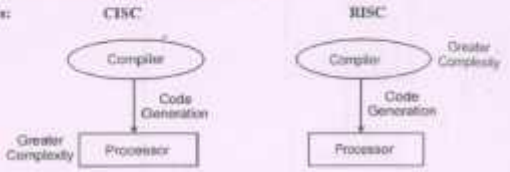
Ans:	*User Mode*	*Exception Mode*
	1) Normal program execution mode.	1) Entered upon execution.
	2) System resources unavailable.	2) Full access to system resources.
	3) Mode changed by exception only.	3) Mode changed freely.

5. **What are the different type of ARM Registers?**

Ans: 1) 31 general purpose 32-bit registers
2) 16 visible R0 - R15
3) Other speed up the exception process

6. What is the difference between CISC and RISC?

Ans:



7. What are the different types of ARM busses?

Ans: (a) AMBA:

(i) Open standard

(ii) Many external devices.

(b) Two Varieties:

(i) AMBA high performance bus (AHB)

(ii) AMBA peripherals bus (APB).

8. What is meant by exception priorities?

Ans: (a) Reset

(b) Data abort

(c) FIQ

(d) IRQ

(e) Prefetch abort

(f) SWI, undefined instruction.

Highest Priority

9. List the various ARM data types?

Ans: (a) 32 bit word.

(b) Word can be divided into four 8-bit bytes.

(c) ARM addresses can be 32 bits long.

(d) Address refers to byte.

Address 4 starts at byte 4.

10. What are the main parts of the ARM processor?

Ans: The main parts of the ARM processor are:

1) Register File.

2) Booth Multiplier.

3) Barrel Shifter.

4) Arithmetic Logic Unit (ALU)

5) Control Unit

11. What is meant by RISC?

Ans: A Reduced Instruction Set Computer (RISC) is a microprocessor that has been designed to perform a smallest of instructions, with the aim of reducing the overall speed of the processor. The RISC concept first originated in the early 1970's when an IBM research team proved that 20% of instruction did 80% of the work. The RISC architecture follows the Philosophy that one instruction should be performed every clock cycle.

12. How would you load the two's complement representation of -1 into register 3 using one instruction?

Ans: MOVN r6, # 0.

13. Implement an ABS (absolute value) function for a registered value using only two instruction?

Ans:

```
MOVS    r7,r7       ;   set the flags
RSBMI   r7,r7,# 0   ;   if neg, r7 = 0 – r7.
```

14. Multiply a number by 35, guaranteeing that its executes in 2 core clock cycles.

Ans:

```
ADD     r9, r8, r8, LSL # 2 ;   r9 = r8 * 5
RSB     r10, r9, r9, LSL # 3 ;  r10 = r9 * 7.
```

15. Draw the ARM based system.

Ans:

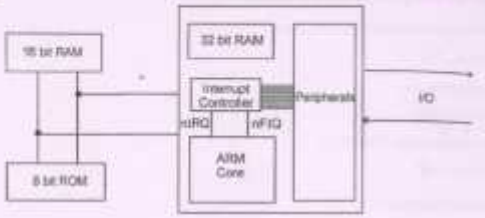


Fig.

16. List some instruction for single register data transfer.

Ans: LDR STR → Word

LDRB STRB → Byte

LDRH STRH → Half Word

LDRSB → Signed Byte Load

LDRSH → Signed half word load.

17. What is the function of Reset?

Ans: When the nRESET signal goes Low, ARM7 abandons the executing instruction and then continues to fetch instructions from incrementing and addresses.

When nRESET goes high again, ARM7 does the following:

(1) Forces M [4:0] = 10011 (Supervisor Mode) and sets the I and F bits in the CPSR.

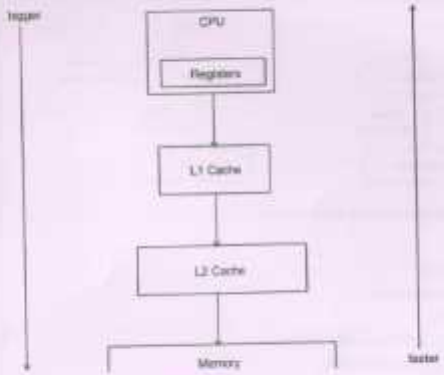
(2) Forces the PC to fetch the next instruction from address 0 X 0 0.

18. What is the role of software interrupt?

Ans: The Software Interrupt Instruction (SWI) is used for getting into Supervisor Mode, usually to request a particular supervisor function when a SWI is executed.

19. Draw the diagram for memory hierarchy?

Ans:



20. Give details about Memory Hierarchy.

Ans: a) processor registers : ~100 bytes, 1 ns.

b) on-chip cache or RAM : ~10 kbytes, 5 ns.

c) off-chip ROM and RAM : ~Mbytes, 50 ns.

d) backup store : ~Gbytes, 5 ms.

21. What is the role of Exceptions?

Ans: Exceptions are usually used to handle unexpected events which arise during the execution of a program.

22. Write example for data processing instructions.

Ans: SUB r0, r1, # 5

ADD r2, r3, LSL # 2

ADDEQ r5, r5, r6.