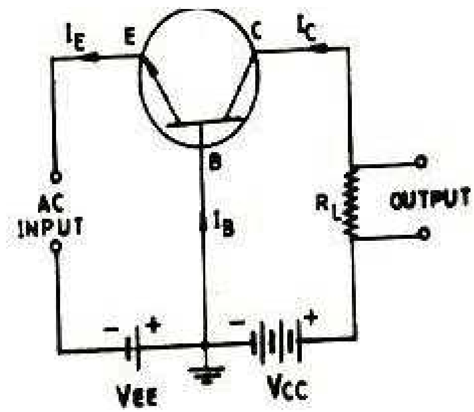
UNIT-II - TRANSISTORS

1. **Calculate β of a transistor when α = 0.98**

   $B = \alpha/1-\alpha = 0.98/1-0.98 = 49$

2. **Among CE,CB and CC configurations, which one is the popular? Why?**
   - ➔ The CE configuration is widely used because it provides both voltage gain as well as current gain greater than unity.

3. **Draw the circuit of NPN transistor in CB configuration?**



4. **What are power transistors? List it's applications.**
   - ➔ Power transistors are designed for power amplification which means that the operating voltage and must be large.

   Applications:

   1. They are used in switching power supplies.
   2. They are used in audio power amplifiers.

5. **What is the relation between IB,IE and IC in CB configuration?**

   Emitter current IE=IB+IC

6. **Name the operating modes of a transistor?**

   1.Cut off
   2.Active
   3.Saturation

7. **What are hybrid parameters**

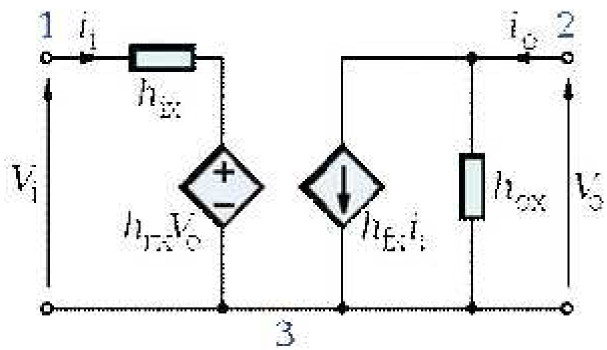
   $h_{11}= Vi/Ii|\ V_0 = 0$ $\qquad h_{21} = I_0/I_i|V_0=0$

   $h_{12} = Vi/V_0|\ I_0 = 0$ $\qquad h_{22} = I_0/V_0|Ii=0$

8. What is the application of optocoupler?

The application of optocoupler is to provide electrical isolation between input and output circuit.

9. Draw the h-parameter equivalent circuit of a CE BJT configuration?



10. Give the h_{ie} and h_{oe} equations of BJT

$h_{ie} = \Delta V_{BE}/\Delta I_B|V_{CE}$ Constant

$h_{oe} = \Delta I_c//\Delta Vc|I_B$ Constant

11. When does a transistor acts as a switch?

The transistor acts as a switch when it is operated at either cutoff region or saturation region.

UNIT-II

TRANSISTORS.

1. Comparison of D-MOSFET & E-MOSFET (8)

S.No.	Enhancement MOSFET	Depletion MOSFET.
1.	Gate - +ve	Gate - Ive.
2.	Channel - Not diffused	Channel - diffused
3.	Drain current ↑ with ↑ in gate vge.	Drain current ↓ with ↓ in -ve gate voltage.
4.	Both P-N channel exist	Both P-N-channel exist
5.	E-type can't be used as D-type	D-type can be used as E type
6.	$I_D \to$ negligible, $V_{GS} = 0$	I_D - consider at $V_{GS} = 0$.
7.	Useful in switching application	less prefered.

2) Compare the following N-channel & P-channel MOSFET (8)

S.No	N-channel MOSFET	P-channel MOSFET.
1.	ON resistance - small, occupies less space.	ON resistance - high. mobility of electrons is 2½ of holes
2.	Size small, C_T - small.	size → greater, C_T reduces speed
3.	+ve gate drain supply	-ve gate drain.
4.	costlier.	cheaper.
5.	saturation region ($V_{DS} > V_{DS(sat)}$)	Saturation region $V_{SD} > V_{SD(SAT)}$
6.	Non " " ($V_{DS} < V_{DS(sat)}$)	Non " " $V_{SD} < V_{SD(SAT)}$
7.	Transition point $V_{DS} = V_{GS} - V_{TN}$	$V_{SD} = V_{SG} + V_{TP}$.

3) Explain the beaising technique of JFET. (16)

* Necessary to maintain the operating point Q stable in the central portion of the pinch off region. V_{GS} & I_D - biasing
* Combination of self bias & fixed bias to provide stability.

8. Explain the working of LCD seven segment display using square wave supply (8).

* LCD - liquid crystal Display are used for display of numeric & alpha-numeric character in dot-matrix and segment displays. (2)

* Construction - two types. (i) Dynamic scattering type (1)
  (ii) field effect type (1)

* Working (2) * Diagram (2)

9. Explain Insulator, Semiconductor & conductor with help of Energy band structure (8) Diagram of Energy bands (2)

Insulator (2): which 8 valence electrons & are bound tight to parent atom

* eg (paper, mica etc.).
* Properties → conductivity, melting & boiling temp ↑

Conductor (2): Electron at outermost orbit of an atom moves freely.

* Properties - conductivity, melting & boiling temp ↓
* eg (copper, iron etc.)

Semiconductor (2): 4 valence electrons, b/w insulator & conductor.

* Properties → conductivity -, melting & boiling temp.
* Eg (silicon, germanium etc.)

10. Write down the expression for transient capacitance & diffusion capacitance (8)

Transition capacitance (4) (C_T) :

* Reverse bias - majority carries more
* Depletion layer widens.
* $C_T = \left|\frac{dQ}{dV}\right|$ (i) Alloy junction (ii) Grown junction

Diffusion capacitance (4) (C_D) :

* $C_T = q \cdot N_D \cdot A \left(\frac{\varepsilon}{q N_D W}\right)$; $C_T = \frac{\varepsilon A}{W}$

* Injected charge storage near the junction
* $C_D = \tau \cdot g$; $C_D = \frac{\tau I}{\eta V_T}$
* for reverse bias, C_D - neglected
* for forward bias, $C_D > C_T$

* Self bias diagram (1) V_{DD} applied, I_D flows in absence of V_G.

$V_S = I_D R_S$ $V_D = V_{DD} - I_D R_D$.

Drain to Source voltage : $V_{DS} = V_{DD} - I_D (R_D + R_S)$

Gate to source Voltage : $V_{GS} = - I_D R_S$.

$I_D \uparrow$, voltage drop $\uparrow$. $\uparrow V_{GS}$, $\downarrow$ width of channel, $\rightarrow \downarrow I_D$

$I_D \downarrow \rightarrow V_{GS} \downarrow$, $\uparrow$ width of channel $\uparrow I_D$.

* Voltage divider bias : $V_{GG} = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD}$; $R_g = \frac{R_1 R_2}{R_1 + R_2}$

diagram (1) $V_{GG} >> V_{GS}$. $I_D \simeq$ Constant.

V_{GS} can vary several volts from one JFET to another.

4. Explain the construction & characteristics of JFET (16).

Construction (8) : FET consists of p-type (or) N-type silicon bar containing two PN junction at the sides.

Notation : Gate (G), Drain (D), Source (S) channel.

Source & Drain may be interchanged.

Diagram for N-channel FET

$I_S, I_D, I_G \rightarrow$ +ve direction

N-channel : V_{DS} – +ve, V_{GS} –ve.

Diagram for p-channel FET.

direction of arrow $\rightarrow$ gate junction

p-channel : I_D, V_{DS} – ve

V_{GS} +ve.

* When V_{GG} applied & $V_D = 0$. – depletion region.
* When V_{DD} applied & $V_{GG} = 0$
* When V_{DD} & V_{GG} applied. – pinch off voltage.

Characteristics of JFET (8) Relate the current & voltage

Transfer Characteristics (4)

I_D, V_{GS} & V_{DS} $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

Drain characteristics (4)

V_{DS} & I_D

Diagram

5. Explain the construction & Characteristics of E_MOSFET (16)

Construction (8) : → No depletion mode.

→ Operated with +ve gate to source voltage V_{GS}.

→ $V_{GS} = 0$, V_{DD} → tries to force electron from source to drain

→ No drain current $V_{GS} = 0$.

* Diagram ; → Inversion layer.

→ Minimum Gate to source voltage → Threshold voltage.

* $V_{GS} < V_{GS(th)}$ → No current flows from D to S

* $V_{GS} > V_{GS(th)}$ → value of current.

characteristics (8) (i) Drain characteristics (4) (ii) Transfer characteristics (4)

diagram → V_{GS} Vs I_D curve & V_{GS} Vs I_{DSS} curve.

I_D ↑ with ↑ in V_{GS}. $I_D = k\left[V_{GS} - V_{GS(th)}\right]^2$ $V_{GS} = 0$.

6. Explain the construction & characteristics of D_MOSFET (16)

Construction (8) : operate in two diff. modes → Depletion & Enhancement mode.

Depletion mode (4) : -ve gate voltage depletes the channel of free electron

diagram

Enhancement mode (4) : V_{GS} → +ve. ↑ the no. of free electron enhance the conduction of channel.

diagram.

Characteristics (8) : .

Drain characteristics (4) : Above $V_{GS} = 0$ +ve, below -ve.
⇓ Enhancement mode ↳ depletion mode.

$V_{DS} = 0$. No conduction.

$V_{GS} > 0$, gate induce more electrons

Transfer characteristics (4) : V_{GS} extends. I_{DSS} → D to S with $V_{GS} = 0$

$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$ Normally ON mosfet. $V_{GS} > 0$, I_D ↑.

7. Explain the biasing characteristics of MOSFET. (16)

Biasing the Enhancement MOSFET (8): Drain to gate bias

* diagram ; $V_{GS} = \left[\frac{R_1}{R_1+R_F}\right] V_{DS}$. DC stabilisation through R_F. I/p R is reduced.

D.C stability by D.C feedback thro R_S.

$V_{GS} = \left(\frac{R_2}{R_1+R_2}\right) V_{DD}$. $V_{GS} = V_{DD} - V_G$

* $V_{GS} > T_N$, $I_D = K_N (V_{GS} - V_{TN})^2$; $V_{DS} = V_{DD} - I_D R_D$.

$V_{DS} > V_{DS(sat)}$ → Saturation region

$V_{DS} < V_{DS(sat)}$ → Non-saturation " ∴ $I_D = K_N[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2]$

Biasing of depletion MOSFET (8):

Biasing the self & voltage bias circuit given for JFET used to establish operating point. Diagram

* self bias (4): $V_{GS} = -I_D R_S$; $V_{DS} = V_{DD} - I_D (R_D + R_S)$

* Voltage divider bias (4): $V_{GG} = \left(\frac{R_2}{R_1+R_2}\right) V_{DD}$. $V_{GS} = V_{GG} - I_D R_S$.

8) Explain the working & principle of operation of UJT & mention its application (16).

UJT - UniJunction Transistor

→ Only one PN junction

* 3 terminal silicon diode

* Ability to control large ac power with small signal I/p.

* -ve resistance char. which use on oscillator.

Principle (2) Operation (2)

Construction (2) diagram (2)

Working (4)

Application (4)

* Intrinsic stand off ratio $\eta = \frac{R_{B1}}{R_{B1}+R_{B2}} = 1$

→ When no voltage is applied to emitter

→ When +ve " " " " "

→ VI - characteristics of UJT: I_E Vs V_E. * Valley point. Saturation region.

Application: switching ckt, pulse generation, timing & trigger ckts

9. Explain the working and characteristics of SCR and its application (16)

SCR - Silicon Controlled Rectifier → Four layered PNPN device

* Used as switching device.

Construction: diagram; Anode, Cathode, Gate.

Biasing: J_1 & J_2 → forward bias which J_2 → Reverse bias.

Operation: * load in series with anode, gate open. No vge.

* Cutoff state
* Anode voltage ↑ to breakover voltage ON state.
* OFF state → No current flow through the device.
* called as Unidirectional device.

V-I characteristics: * forward: $I_G = 0$ (forward blocking region, conduction ")

* Reverse : :

Application: relay controls, static switches, heater control etc,

10. Briefly explain the operation of TRIAC & DIAC (16)

TRIAC - Triode A.C switch → three terminal semiconductor switch (8)

(diagram & Characteristic curve)

* MT_1, MT_2 & gate.
* Equivalent to 2 SCR in parallel but in reverse direction
* leakage current - small.
* Device - start conducting → high current flow.
* Bidirectional device.
* Used for illumination, temperature control.

DIAC (8) - Diode A.C switch - 3 layer 2 terminal device

* Not a control device.
* Used as triggering device.

* MT_1, MT_2. Bidirectional avalanche diode
* Identical chars for +ve & -ve half of a.c
* Vge < breakover voltage ∴ Current small.
* reaches breakover, exhibit -ve resistance
* Current ↑, voltage decreasing.