	Sri Vidya College of Engineering And Technology **Virudhunagar – 626 005** **Department of Electrical and Electronics Engineering**	

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Subject Code/ Name: EE6301/ DIGITAL LOGIC CIRCUITS

UNIT IV -ASYNCHRONOUS SEQUENTIAL CIRCUITS

PART-A

1. Define state of sequential circuit.
The binary information stored in the memory elements at any given time defines the "state" of sequential circuit.

2. Define fundamental mode .
Only one input variable can change at any one time and the time between two inputs changes must be longer than the time it takes the circuit to reach a stable state.

3. What is meant by state reduction?
The reduction of number of flip flops in a sequential circuit is referred as state reduction problem. The state reduction algorithms are concerned with procedures for reducing the number of states in a state table while keeping the external input – output requirements unchanged.

4. Mention the application areas of asynchronous sequential circuits.
i. Used where speed is important,(i.e.) where the digital system must respond quickly without the need to wait for clock pulse.
ii. Require only few components (i.e) no need for additional clock pulses.
iii. Used where the input change at any time independent of clock.
iv. Communication between two units where each has own independent clock.

5. Mention the faults in asynchronous sequential circuits.
(1)Hazards (2) Oscillations (3) Critical races

6. Define secondary variables of asynchronous sequential circuits.
The present state and the next state variables in asynchronous sequential circuits are called Secondary / excitation variables.

7. What do you mean by race in asynchronous sequential circuits?
When two or more binary state variables change their value in response to a change in an input variable, race condition occurs in an asynchronous sequential

circuit. In case of unequal delays, a race condition may cause the state variables to change in an unpredictable manner.

8. Define critical race in asynchronous sequential circuits.
If the final stable state depends on the order in which the state variables changes, the race condition is harmful and it is called a critical race. This should be avoided.

9. Define non-critical race
If the final stable state that the circuit reaches does not depend on the order in which the state variables changes , the race condition is not harmful and it is called a noncritical race.

10. Define Hazard & Name the types of hazards
Hazard is unwanted switching transients that may appear at the output of a circuit because different paths exhibit different propagation delays. Static hazard, Dynamic hazard, Essential hazard.

11. What is a glitch?
These glitches are very narrow pulses, often having a width of a few nano seconds that occur during the switching of variables.

12. Define Static hazard & Dynamic hazard.
In a combinational circuit, if the outputs before and after change of input are the same then the hazard is called a static hazard.If the output before and after the change of input are different and the output changes three times instead of once and passes through an additional temporary sequence of 0 1 or 1 0 in going to the final output.

13. Define Essential hazard.
An essential hazard is caused by unequal delays along two or more paths that originate from the same input. Such hazards can be eliminated by adjusting the amount of delays in the affected path.

14. What is a flow table & primitive flow table?
During the design of asynchronous sequential circuits, it is more convenient to name the states by letter symbols without making specific reference to their binary values. Such a table is called a flow table. primitive flow is the flow table that has only one stable state in each row.

15. What is static 0 and 1 hazard?

Static 1 hazard – if the outputs before and after the change of input are both 1 with an incorrect output 0 in between.

Static 0 hazard - if the outputs before and after the change of input are both 0 with an incorrect output 1 in between.

16. Mention the algorithm for state reduction.
Two states are said to be equivalent if, for each member of the set of inputs, they give exactly the same output and send the circuit to an equivalent state. When two states are equivalent, one of them can be removed without altering the input – output relationships.

17. How will you avoid the race conditions in asynchronous sequential circuits?
Races may be avoided by proper binary assignment to state variables. The state variables must be assigned binary numbers in such a way that only one state variable can change at any one time when a state transition occurs in the flow table.

18. What is meant by cycles in asynchronous sequential circuits?
Races can be avoided by directing the circuits through intermediate unstable states with a unique state variable change. When a circuit goes through a unique sequence of unstable states , it is said to have a cycle.

19. Mention the excitation function for SR latch using NOR & NAND gates.
Nor gate :Y = S+R‟y When SR = 0
NAND gate :Y = S‟ + Ry

20. What are the steps to be followed for the purpose of merging a flow table?
(1) Determine all compatible pairs by using the implication table.
(2) Find the maximal compatibles using a merger diagram.
(3) Find a maximal collection of compatibles that covers all the states and is closed.

21. What is meant by compatible pairs?
Two states are said to be compatible, if in every column of the corresponding rows in the flow table, there are identical states and if there is no conflict in the output values.

22. What is maximal compatibles?
The maximal compatible is a group of compatibles that contains all the possible combinations of compatible states.

23. What is the use of merger diagram?
The maximal compatibles can be obtained from a merger diagram which is a graph in which each state is represented by a dot placed along the circumference of a circle. Lines are drawn between any two corresponding dots that form a

compatible pair. All possible compatibles can be obtained from the merger diagram by observing the geometrical patterns in which states are connected to each other.

24. How will you remove the hazards in combinational logic circuits?
It can be removed by covering any two minterms that may produce a hazard with a product term common to both. The removal of hazards requires the addition of redundant gates to the circuit.

25. Compare Synchronous counters and Asynchronous counters.

S.no	Asynsynchronous counters	Synchronous counters
1.	Flipflops are connected in such a way that the output of first flipflop drives the clock for the next flipflop	There is no connection between the output of first flipflop and clock input of the next flipflop.
2.	All the flipflops are not clocked simultaneously.	All the flipflops are clocked simultaneously.
3.	Logic circuit is simple even for more number of states.	Design involves complex logic circuit as number of states increases.
4.	Main drawback of these counters is their low speed as the clock is propagated through number of flipflops before it reaches last flipflop.	As clock is simultaneously given to all flipflops there is no problem of propagation delay. Hence they are preferred when number of flipflops increase in the given design.

26. What is the form in which the information is stored in memories?
It is stored in the form of voltages corresponding to logic 0 and logic 1, i,e., in the binary form.

27. What are the main advantages of semiconductor memories over magnetic memories?
Small size, low cost, high reliability, case of expansion of memory size, and electrical compatibility with the microprocessors.

28. What happens to the information stored in a memory location after it has been read & write operation?

The reading operation is non-destructive, which, means the stored information remains intact and can be read any number of times. The previously stored information automatically gets erased and new information is stored.

29. Differentiate between the random-access memory and the sequentia memory from the point of view of speed of operation.
The access time is same for every memory location in the case of random- access memory, whereas it is different for different memory location in the case of sequential memory. Therefore, the random-access memory is faster than sequential memory.

30. How erasing operation is performed in the EPROM?
For erasing the EPROM it is exposed to ultraviolet radiation for the specified time duration.

31. What is meant by dynamic RAMs and dynamic RAMs require refreshing?
The memory cells of dynamic RAMs are basically charge storage capacitors with driver transistors. The presence or absence of charge in a capacitor is interpreted as logical 1or 0.Because of the charge‟s natural tendency to distribute itself into a lower energy-state configuration (i.e., the charge stored on capacitors leak – off with time), dynamic periodic charge refreshing to maintain data storage.

32. What is the basic memory cell used in static RAMs ? Does it require refreshing?

Static RAMs store ones and zeros using conventional flip-flops. These do not require refreshing because there is no problem of charge leaking-off in flip – flops.

33. What are the advantages of dynamic RAMs over static RAMs?
(i) Higher number of bits storage on a given siliconchip area, i,e, higher packaging density .
(ii) Lower power consumption.

34. What are advantages of static RAMs over dynamic RAMs?
(i) Higher speed of operation (faster),
(ii) Does not require refreshing.

35. Which is the type of memory preferred for the storage of program in a microcomputer and why? Read – only memories are preferred for program storage because these are non-volatile.

36. What are the performance characteristics used to compare semiconductor technologies used for making memories?

Density, i.e. the number of memory location on a given silicon area.

Speed of operation, i,e., the access time.

Power consumption.

Cost\bit.

37. Compare Static RAM and Dynamic RAM

Static RAM

It contains less memory cells per unit area.

It has less access time hence faster memories

It consists of number of flip-flops, each flip-flop stores one bit.

Refreshing circuitry is not required.

Cost is more.

Dynamic RAM

It contains more memory cells per unit area as compared to Static RAM

Its access time is greater than static RAMs

It stores the data as a charge on the capacitor. It consists of MOSFET and the capacitor for each cell.

Refreshing circuitry is required to maintain the charge on the capacitors after every few milliseconds. Extra hardware is required to control refreshing. This makes system design complex.

Cost is less.

38. What do you mean by programmable logic devices?

Programmable logic devices (PLD) are an integrated circuit with internal logic gates that are connected through electronic fuses. It consists of AND array and OR array that are connected together to provide a sum of product implementation. The initial state of a PLD has all the fuses intact. Programming

the device involves the blowing of internal fuses to achieve a desired logic function.

39. What is the advantage of using PLD‟s in the design of digital systems?

PLD‟s can be programmed to incorporate complex logic functions within one LSI circuit. It is also an alternative to another design technology called VLSI design.

40. What is ROM and What are the types of ROM‟s?

A Read only memory is a device that includes both the decoder and the OR gates within a single IC package. The connections between the outputs of the decoder and the inputs of the OR gates is specified for each particular configuration. The ROM is used to implement complex combinational circuits within one IC package or as permanent storage for binary information.Mask Programmable ROM‟s, Field Programmable ROM‟s (PROM), Erasable Programmable ROM‟s (EPROM).

41. What is Programmable ROM‟s (PROM)?
Programmable ROM has a fixed AND array and programmable fuses for the output OR gates.

42. What is Programmable Logic Array?

Programmable logic array has both AND and OR array to be programmed. The product terms in the AND array may be shared by any OR gate to provide the required sum of products implementation.

43. Compare PROM, PLA and PAL.
PROM:
(1) AND array is fixed, OR array programmable
(2) Cheaper and simpler to use
(3) Only Boolean functions in standard SOP form can be implemented.
PLA:
(1) Both AND and OR array are programmable
(2) Costly and complex
(3) Any Boolean functions in SOP form can be implemented.
PAL:
(1) OR array is fixed and AND array is programmable
(2) Cheaper and simpler
(3) Any Boolean functions in SOP form can be implemented

44.What are the different types of programming the PLA?
i. Mask programmable – the customer must submit a PLA program table to the manufacturer. This table is used by the vendor to produce the custom made PLA that has required paths between inputs and outputs.

ii. Field programmable – it can be programmed by the user under certain recommended procedures.

Unit IV

1. When does oscillation occur in an asynchronous sequential logic ckt ?

In an asynchronous m/c a race condition is said to have occured if two or more state variables change their values when there is a state transition.

Races
- Non critical Race
- Critical Race

Non critical race → not harmful

Critical race → harmful

2. Draw & explain the state transition diagram of Modulo – 6 counter in asynchronous sequential logic

Present state				Next state			Stable	output
E	X_3	X_2	X_1	X_3^+	X_2^+	X_1^+	Yes/No	Z
0	0	0	0	0	0	1	Yes	0
0	0	0	1	0	1	0	Yes	0
0	0	1	0	0	1	1	Yes	0
0	0	1	1	1	0	0	Yes	0
0	1	0	0	1	0	1	Yes	0
0	1	0	1	1	1	0	Yes	0
0	1	1	0	1	1	1	Yes	0
0	1	1	1	0	0	0	Yes	0
1	0	0	0	0	0	1	No	0
1	0	0	1	0	1	0	No	0
1	0	1	0	0	1	1	No	0
1	0	1	1	1	0	0	No	0
1	1	0	0	1	0	1	No	0
1	1	0	1	1	1	0	No	0
1	1	1	0	1	1	1	No	1
1	1	1	1	0	0	0	No	0

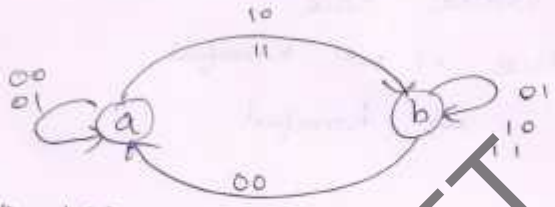
$$X_3^+ = X_3\bar{X}_2 + EX_3 + E\bar{X}_3X_2\bar{X}_1$$

$$X_2^+ = X_2\bar{X}_1 + \bar{X}_3X_2$$

$$X_1^+ = \bar{E}\bar{X}_2X_1 + \bar{E}\bar{X}_3X_1 + E\bar{X}_2\bar{X}_1 + E\bar{X}_3\bar{X}_1$$

$$Z = EX_3X_2\bar{X}_1$$

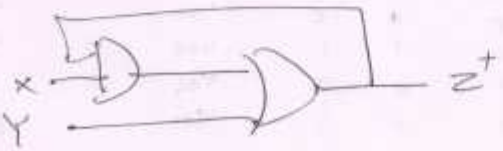
3. Design an asynchronous seq. logic ckt for the state & transition diagram.



Transition table

P.S	N.S			
	00	01	11	10
a	a	a	b	b
b	a	b	b	b

$$z^+ = x + yz$$



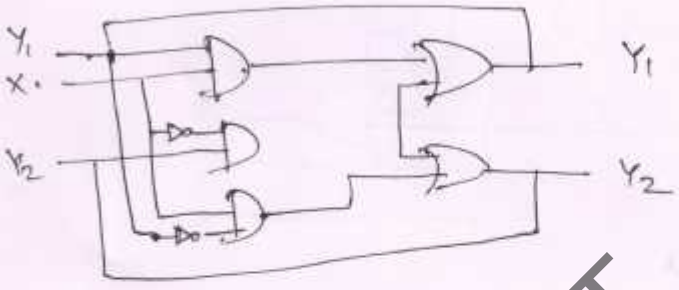
4. Discuss about the programmable logic gates.

1. Simple programmable logic devices (SPLD)
   - (a) PROM
   - (b) PLA
   - (c) PAL
   - (d) GAL

2. CPLD (Complex Programmable logic devices)

3. FPGA (Field Programmable Gate Array)

5. Derive the transition table and primitive flow table for the functional mode asynchronous seq. ckt shown.



$Y_1 = xy_1 + x'y_2$

$Y_2 = xy_1' + x'y_2$

Transition Table

Y_1Y_2 \ x	0	1
00	(00)	01
01	11	(01)
11	(11)	10
10	00	(10)

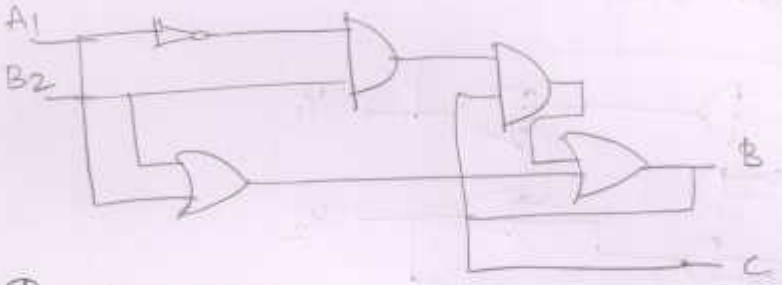
Y_1Y_2 \ x	0	1
00	(a)	b
01	c	(b)
11	(c)	d
10	a	(d)

6 Illustrate the analysis procedure of asynchronous seq. ckt with an example.

Let $B = (\bar{A}_1 B_2) B + (A_1 + B_2)$

$B = C$

Logic diagram



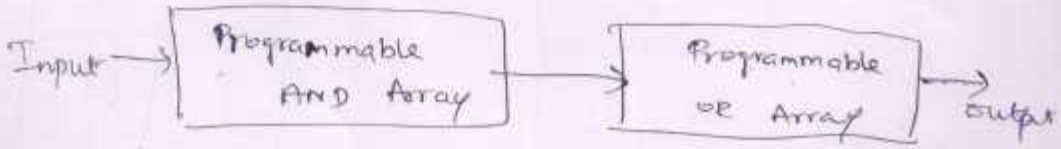
Transition table

B	A1B2 = 00	01	11	10
0	(0)	1	1	1
1	0	(1)	(1)	(1)

Output map

B	A1B2 = 00	01	11	10
0	0	0	0	0
1	1	1	1	1

7. Illustrate the basic principles of PLA & FPGA



8 Implement the following PLA

$F_1 = \Sigma m (1, 2, 4, 6)$ $F_2 = \Sigma m (0, 1, 6, 7)$

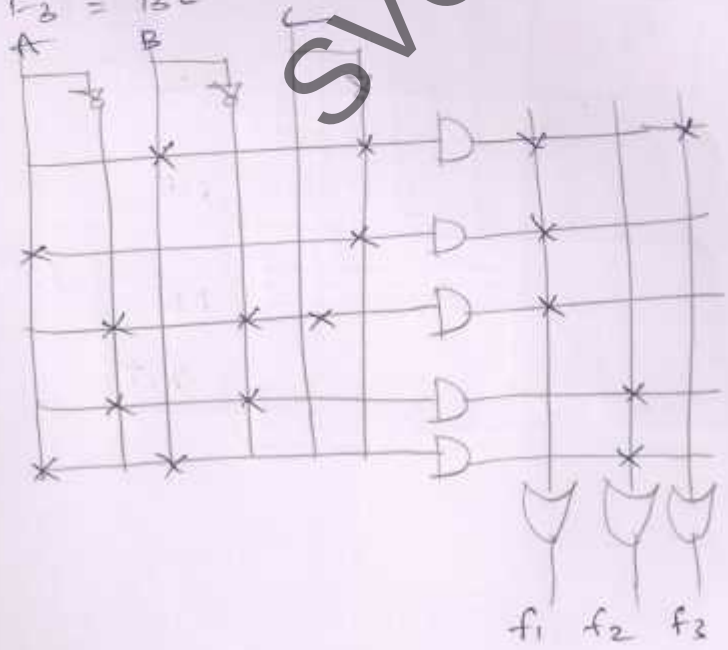
$F_3 = \Sigma m (2, 6)$

A	B	C	F_1	F_2	F_3
0	0	0	0	1	0
0	0	1	1	1	0
0	1	0	1	0	1
0	1	1	0	0	0
1	0	0	1	0	0
1	0	1	0	0	0
1	1	0	1	1	1
1	1	1	0	1	0

$F_1 = B\bar{C} + A\bar{C} + \bar{A}\bar{B}C$

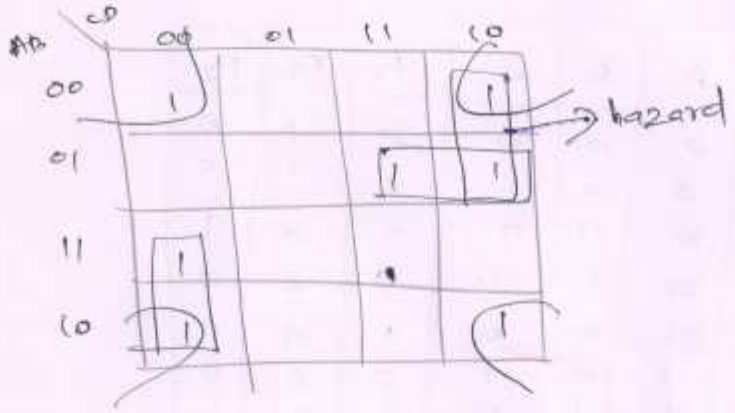
$F_2 = \bar{A}\bar{B} + AB$

$F_3 = B\bar{C}$



9. Find a ckt that has no static hazards and implements boolean fn

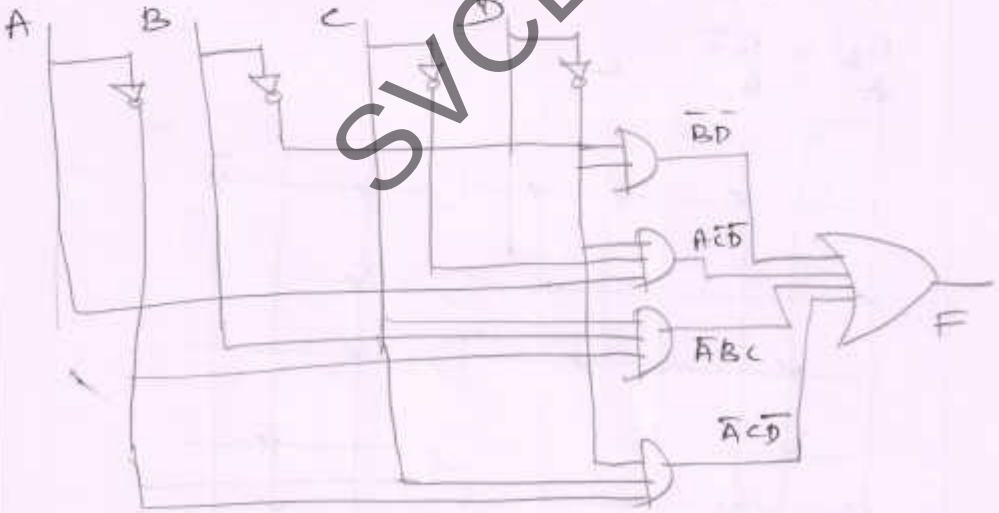
$$F(A,B,C,D) = \Sigma(0,2,6,7,8,10,12)$$



$$F(A,B,C,D) = \bar{B}\bar{D} + A\bar{C}\bar{D} + \bar{A}BC$$

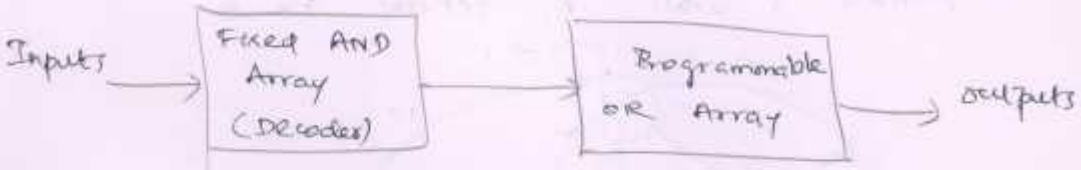
Hazard free realization

$$F(A,B,C,D) = \bar{B}\bar{D} + A\bar{C}\bar{D} + \bar{A}BC + \bar{A}C\bar{D}$$



10 Explain the different types of programmable logic devices with neat schematic and compare them.

PROM :

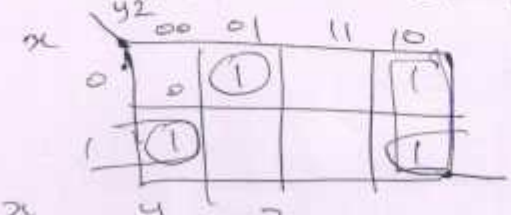


PLD :

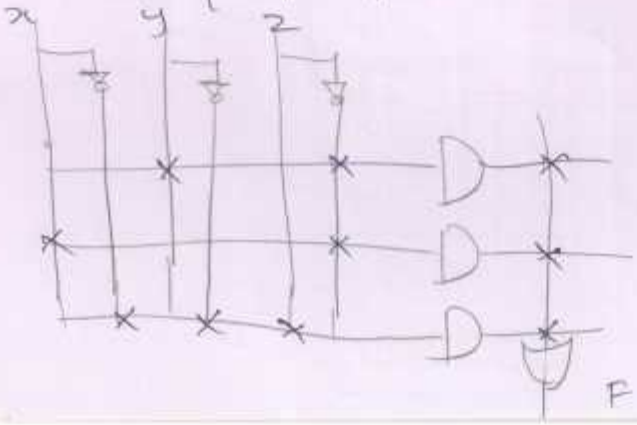
PAL :

11. Implement the following using PLA.

$F(x, y, z) = \sum (1, 2, 4, 6)$



$F = xy\bar{z} + x\bar{z} + \bar{x}yz$



12. Design an asy. seq ckt that has two inputs x_2 & x_1 and one o/p Z. When $X_1 = 0$, the output $Z = 0$. The first change in x_2 that occurs when x_1 is 1 will cause output z to be 1. The output Z will remain 1 until X_1 returns to 0