	Sri Vidya College of Engineering And Technology **Virudhunagar – 626 005** **Department of Electrical and Electronics Engineering**	

Year/ Semester/ Class : II/ III/ EEE Academic Year: 2017-2018

Subject Code/ Name: EE6301/ DIGITAL LOGIC CIRCUITS

UNIT III -SYNCHRONUS SEQUENTIAL CIRCUITS

PART-A

1. What is a sequential circuit 7& List the types of sequential circuit.
The sequential circuit consists of a combinational circuit to which memory elements are connected to form a feed back path. The output at any instant of time depends on the present inputs and past output. Synchronous Sequential Circuit and Asynchronous Sequential Circuit.

2. What do you mean by synchronous sequential circuit & clocked sequential circuits?
A synchronous sequential circuit is a system whose behavior can be defined from the knowledge of its signal at discrete instants of time. Synchronous sequential circuit that uses clock pulses in the inputs of memory elements is called clocked sequential circuit. The change of internal state occurs in response to the synchronized Clock pulses.

3. What is called a latch?
Unclocked flip-flop that responds to pulse duration is called a latch.

4. What is a flip-flop & List the different types of flip-flops.
It is a basic memory element used to store one bit of information. It is also called as a bistable multivibrator. A flip-flop circuit has two outputs, one for the normal value and one for the complement of the bit stored in it. It can store the binary value indefinitely until directed by an input signal to switch states. RS, D, T, J K and J K master slave flip-flop.

5. Name the different types of triggering employed in a flip-flop?
Level triggering and Edge triggering

6. What are the differences between RS latch and edge triggered RS flip-flop?
RS LATCH: 1.No clock pulse input is present

2. Output changes state on the application of inputs

Edge Triggered RS FLIPFLOP:
1. Clock pulse input is present
2.Output changes state only on the transition of clock pulses depending on the input.

7. Give the truth table of RS flip-flop and JK flip-flop.

R	**S**	**Qn+1**		**Qn+1**
0	0	Qn	Qn‟	No change
0	1	1	0	Set
1	0	0	1	Reset
1	1	Forbidden		

J	**K**	**Qn+1**	**Qn+1**	
0	0	Qn	Qn‟	No change
0	1	0	1	Reset
1	0	1	0	Set
1	1	Qn‟	Qn	Toggle

8. What do you mean by race around condition in a flip-flop?
When both J = K = 1 and clock pulse is „1‟ it causes the output to complement again and repeat complementing until the pulse goes back to „0‟(i.e.) the output toggles continuously. This Race condition arises when the width of the clock pulse is greater than the propagation delay time of the flip-flop.

9. What is a master slave flip-flop?
A master slave flip-flop is constructed from two separate flipflops. One circuit serves as a master and the other as a slave, the overall circuit is referred to as a master slave flip-flop. Both the flipflops are positive level triggered but the presence of inverter at the clock input of the slave flip-flop forces it to trigger at the negative level.

10. What is direct preset and clear inputs?

- Preset -used to set the flip-flop in the initial stage.
- Clear- used to clear the flip-flop in the initial stage

11. What is the difference between truth table and excitation table?
A truth table is a table indicating the output of a combinational circuit for all input states.An excitation table is a list of Flip-flop input conditions that will cause the required state transitions.

12. What is a counter?
A Sequential circuit that goes through a prescribed sequence of states upon the application of input pulses is called a counter.

13. Difference between synchronous and asynchronous counter.
Synchronous counter:

- All the flipflops are clocked simultaneously
- No connection between the output of the first flip-flop and the clock input for the next Flip-flop.
- Design involves complex logic circuit as the number of states increases.
- As the clock is simultaneously given to all flipflops there is no problem of propagation delay.

Asynchronous counter:

- All the flipflops are not clocked simultaneously
- The output of the first flip-flop drives the clock input for the next Flip-flop.
- Logic circuit is simple even for more number of stages.
- Main drawback of these counters is their low speed as the clock is propagated through number of flipflops before it reaches the last flip-flop.

14. What is a presettable counter & ripple counter?
Normally the count starts from zero in a counter. A presettable counter is used to start the count from any number other than zero. A ripple counter is an asynchronous counter, in which the output of the flip-flops change state like a ripple in water and hence the name ripple counter.

15. Mention the applications of counter?
They are used for counting the number of occurrences of an event and are useful for generating timing sequences to control operations in a digital systems.They are used as frequency dividers in digital time pieces, such as, electronic digital clocks, Automobile digital clock and wrist watches, frequency counters, and oscilloscope and television receivers.

16. What is a modulo counter, ring and johnson counter?
Modulo „n‟ counter have „n‟ different states that counts from 0 to n-1 by making small changes in a counter circuit.A ring counter is a circular shift register with only one flipflop being set at any particular time, all others are cleared. A johnson /switched tail ring counter is a circular shift register with the complement output of the last flip-flop connected to the input of the first flip-flop.

17. What is a BCD counter?
A BCD counter counts in binary coded decimal from 0000 to 1001 and back to 0000.It is also a decade counter since it counts from 0 to 9.

18. What is a register & a shift register??
A register is group of binary cells suitable for holding binary information. A group of flipflops constitutes a register, since each flip-flop is a binary cell capable of storing one bit of information.A register capable of shifting the binary information either to the right or in the left is called a shift register.

19. What are the types of shift registers?

- Serial in Serial out(SISO) Serial in Parallel out(SIPO)
- Parallel in Parallel out(PIPO) Parallel in Serial out(PISO)

20. Mention the applications of shift registers?
To introduce time delay, Serial to Parallel converter, Parallel to serial converter, Sequence generator, Ring counter.

21. What is sequence generator?
A circuit which generates a prescribed sequence of bits in synchronism with a clock is referred to as a sequence generator.

22. What is a state table, state diagram& state equation?
The table which lists the time sequence of inputs, outputs and flip-flop states. A state diagram is a graphical representation of the information available in a state table. In the diagram, a state is denoted by a circle and the transitions between the states are indicated by directing lines connecting the circles.A state equation (transition equation) specifies the condition for a flip-flop state transition. It denotes the next state as a function of the present state and inputs.

23. Explain mealy model and Moore model.

Moore Model:

Its output is a function of present state only.

Input changes does not affect the output

It requires more number of states for implementing same function.

Mealy model:

Its output is a function of present state as well as present input

Input changes may affect the output of the circuit

It requires less number of states for implementing same function.

24. What is the need for debounce circuit?

It is the one that removes the series of pulses that result from a contact bounce and produces a single smooth transition of the binary signal from 0 to 1 or from 1 to 0.

PART B

Unit III

1. A sequential ckt with 2D FFs A, B and X are Input, Y → output specified by the following next state and output eqns.

$A(t+1) = Ax + Bx$

$B(t+1) = A'x$

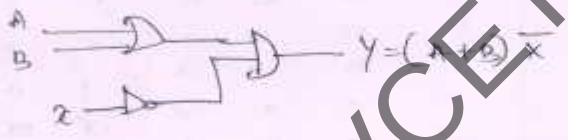
$Y = (A + B)x'$

(i) Draw the logic dia of the ckt

(ii) Derive the state table.

(iii) Derive the state diagram

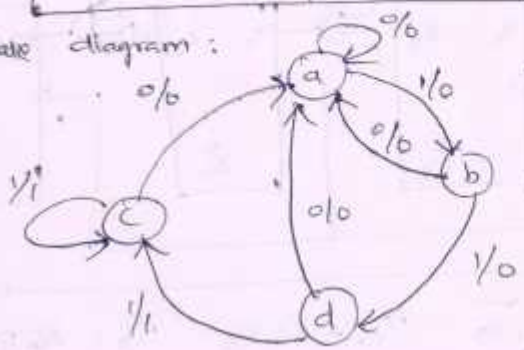
Logic diagram :



State table :

Present state	Next state $x=0$ A^+B^+	Next state $x=1$ A^+B^+	Output (Y) $x=0$	Output (Y) $x=1$
a	a	b	0	0
b	a	d	0	0
c	a	c	0	1
d	a	c	0	1

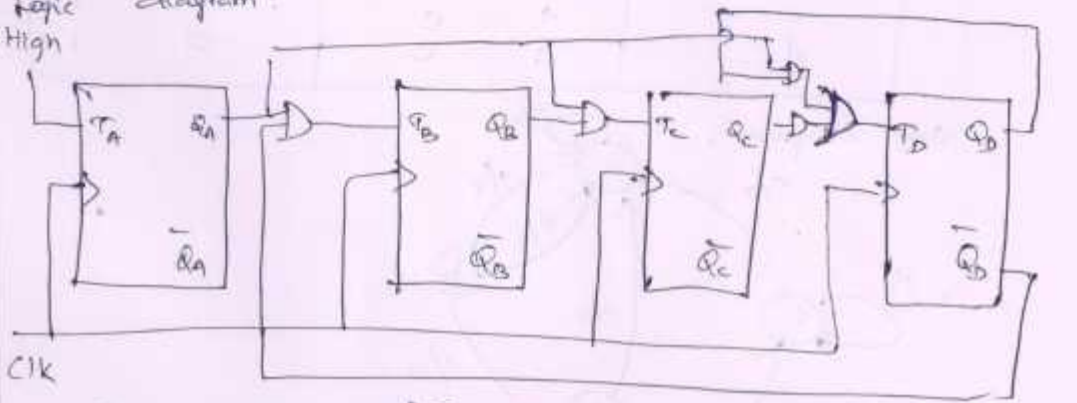
State diagram :



2. Design and implement a synchronous decade counter using T flip flop and construct the timing diagram.

Present state				Next state				Flip flop I/P			
Q_D	Q_C	Q_B	Q_A	Q_{D+1}	Q_{C+1}	Q_{B+1}	Q_{A+1}	T_D	T_C	T_B	T_A
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	1
0	1	0	1	0	1	1	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	1
0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	1
1	0	0	1	1	0	1	0	0	0	1	1
1	0	1	0	1	0	1	1	0	0	0	1
1	0	1	1	1	1	0	0	1	1	1	1
1	1	0	0	x	x	x	x	x	x	x	x
1	1	0	1	x	x	x	x	x	x	x	x
1	1	1	0	x	x	x	x	x	x	x	x
1	1	1	1	x	x	x	x	x	x	x	x

Logic diagram:

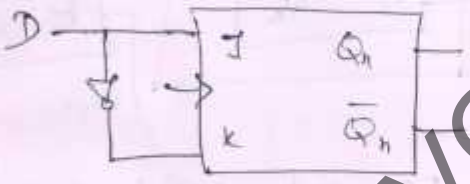


$T_A = 1$ $T_B = Q_A \bar{Q}_D$ $T_C = Q_A Q_B$ $T_D = Q_A Q_D + Q_A Q_B$

3. Show how the JK flip flop can be modified into D flip flop (or) T flip flop.

Input	Present State	Next State	Flip flop I/ps	
D	Q_n	Q_{n+1}	J	K
0	0	0	0	x
0	1	0	x	1
1	0	1	1	x
1	1	1	x	0

$J = D$; $K = \overline{D}$



4. Design MOD-5 Synchronous counter using JK FF.

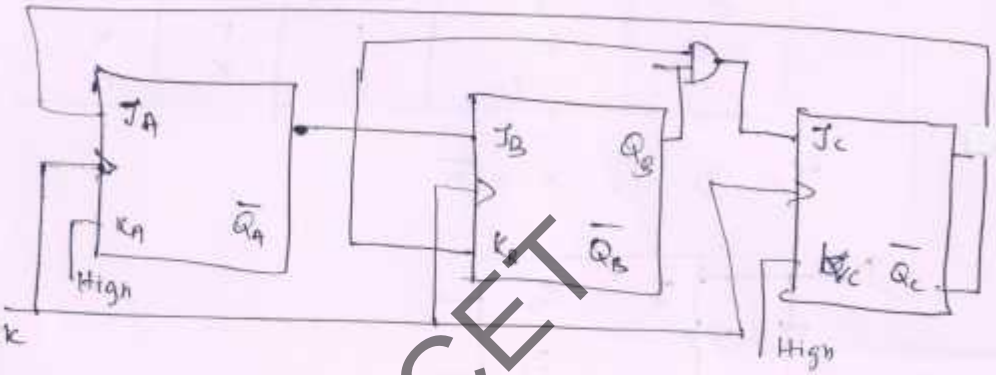
Present State			Next state			Flip flop Inputs					
Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	0	x	1	1	x
0	0	1	0	1	0	0	1	x	x	x	1
0	1	0	0	1	1	0	x	0	1	1	x
0	1	1	1	0	0	1	x	1	x	x	1
1	0	0	1	0	1	x	0	x	0	0	x
1	0	1	x	x	x	x	x	x	x	x	x
1	1	0	x	x	x	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x	x	x	x

$J_C = Q_B Q_A$ $K_C = 1$

$J_B = Q_A$ $K_B = Q_A$

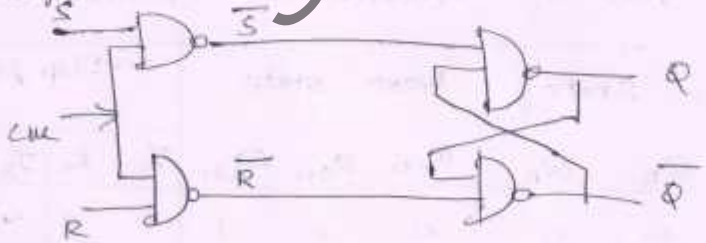
$J_A = \bar{Q}_C$ $K_A = 1$

Logic diagram



5. Explain the clocked SR FF and explain operation.

Logic diagram



Truth tables

CP	S	R	Q_n	Q_{n+1}	State
↑	0	0	0	0	NC
	0	0	1	1	
↑	0	1	0	0	Reset
	0	1	1	0	
↑	1	0	0	1	Set
	1	0	1	1	
↑	1	1	0	X	Indeterminate
	1	1	1	X	
	X	X	0	0	NC

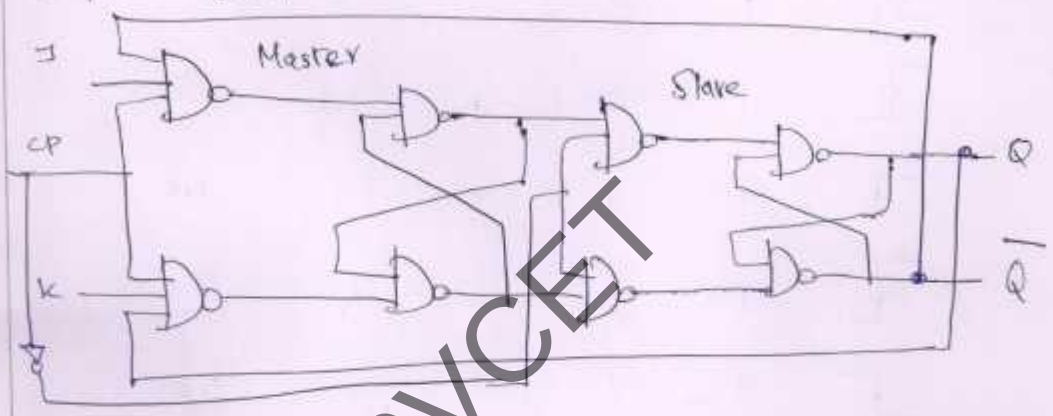
Characteristic table

SR	Q_n	
00		1
01		
11	X	X
10	1	0

$$Q_{n+1} = S + \bar{R} Q_n$$

6. Explain the operation of master slave JK ff.

Logic diagram

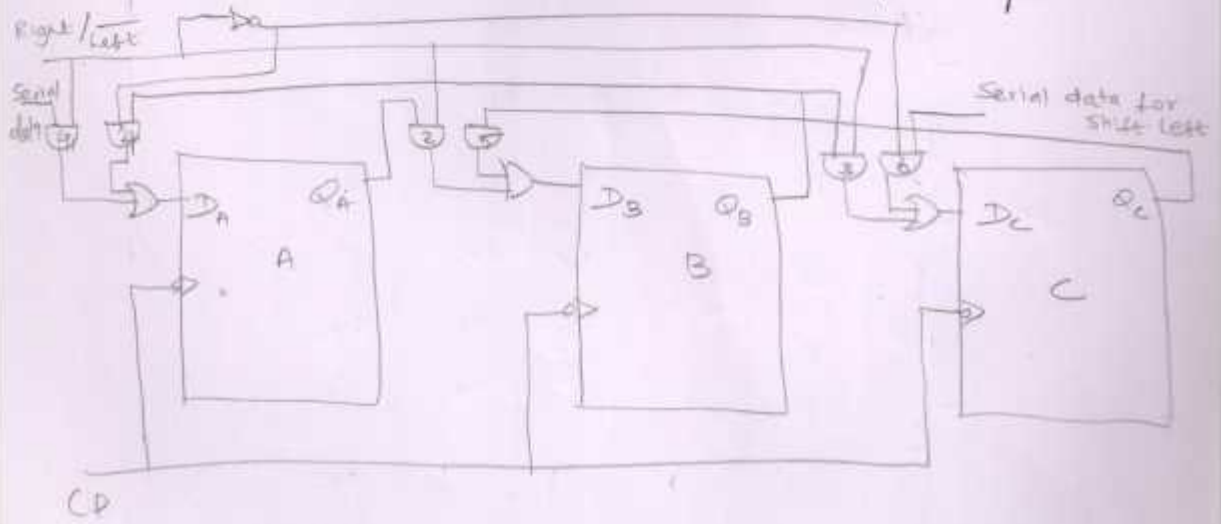


Truth table

CP	Q_n	J	K	Y	Q_{n+1}
↑	0	0	0	0	NC
↓	0	0	0	NC	0
↑	0	0	1	0	NC
↓	0	0	1	NC	0
↑	0	1	0	1	NC
↓	0	1	0	NC	1
↑	0	1	1	1	NC

CP	Q_n	J	K	Y	Q_{n+1}
↓	0	1	1	NC	1
↑	1	0	0	1	NC
↓	1	0	0	NC	1
↑	1	0	1	0	NC
↓	1	0	1	NC	0
↑	1	1	0	1	NC
↓	1	1	0	NC	1
↑	1	1	1	0	NC
↓	1	1	1	NC	0

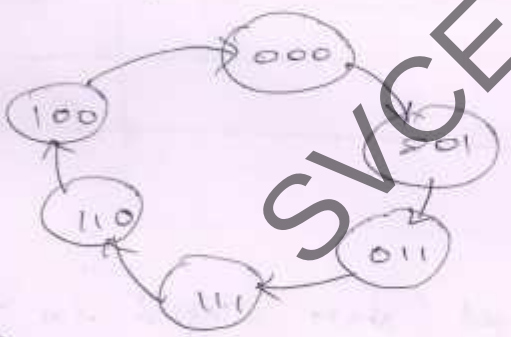
7. Design 3 bit bidirectional shift register.



8. Design a Counter using JK flip flop for realizing the following sequence

Q_2	Q_1	Q_0	
0	0	0	0
0	0	1	1
0	1	1	3
1	1	1	7
1	1	0	6
1	0	0	4
0	0	0	0

State diagram



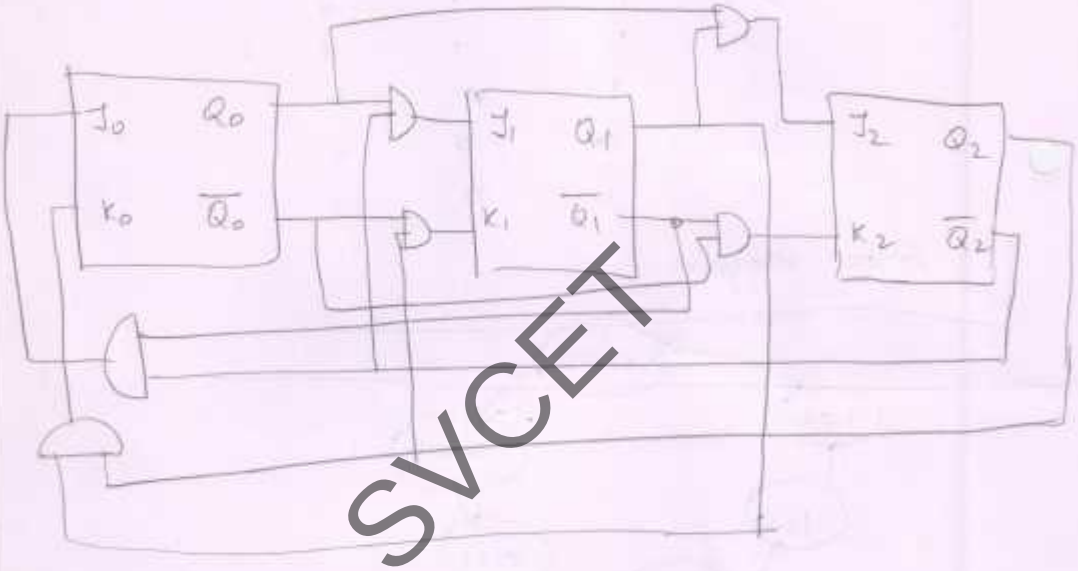
Present state			Next state			JK inputs					
Q_2	Q_1	Q_0	Q_{2+1}	Q_{1+1}	Q_{0+1}	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	1	0	x	1	x	x	0
0	1	1	1	1	1	1	x	x	0	x	0
1	1	1	1	1	0	x	0	x	0	x	1
1	1	0	1	0	0	x	0	x	1	0	x
1	0	0	0	0	0	x	1	0	x	0	x

8. $J_2 = Q_1$ $K_2 = \overline{Q_1}$

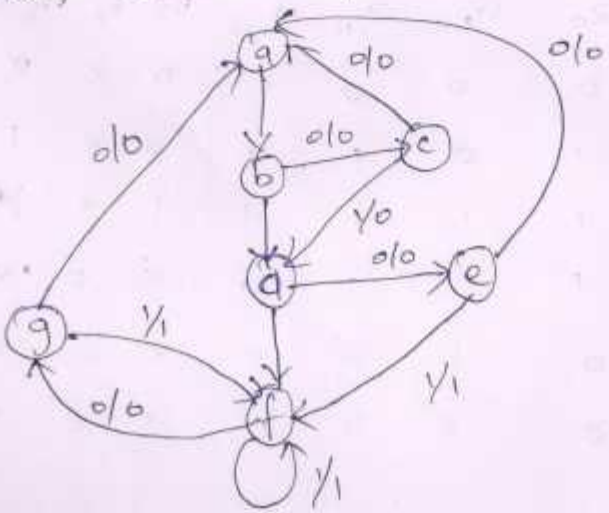
$J_1 = Q_0$ $K_1 = \overline{Q_0}$

$J_0 = \overline{Q_2}$ $K_0 = Q_2$

Logic diagram:



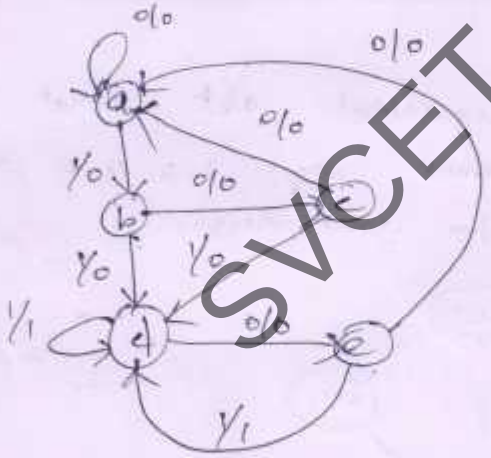
9. Construct reduced state diagram for the following state diagram.



Reduced State table

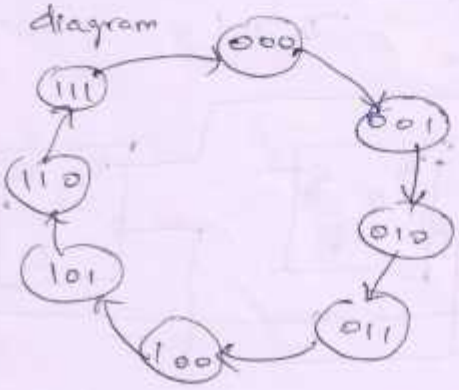
Present State	Next state		output	
	X=0	X=1	X=0	X=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	d	0	1
e	a	d	0	1

Reduced state diagram



10. Design a 3 bit binary counter using T ff

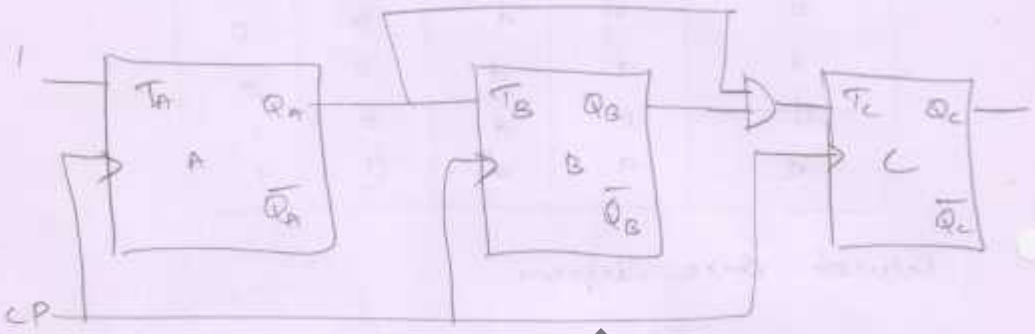
State diagram



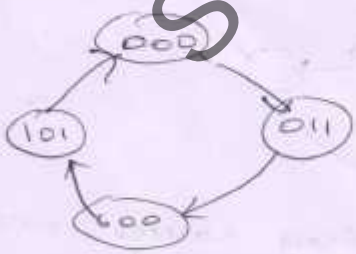
Draw the transition table

$T_C = Q_A Q_B$ $T_B = Q_A$ $T_A = 1$

Logic diagram :

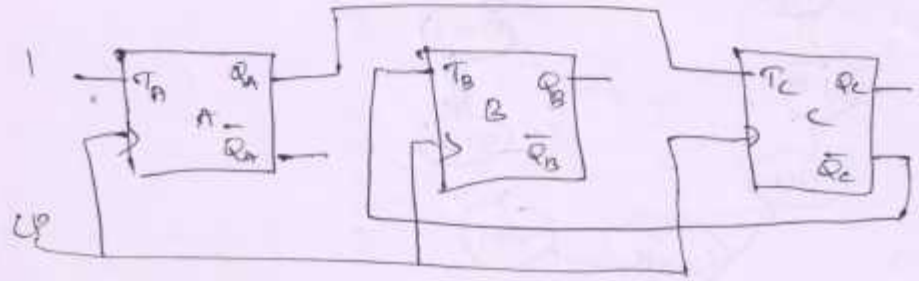


11. Design Syn. sequential ckt that goes through the count seq. 1, 3, 4, 5 repeatly. Use T ff for your design.



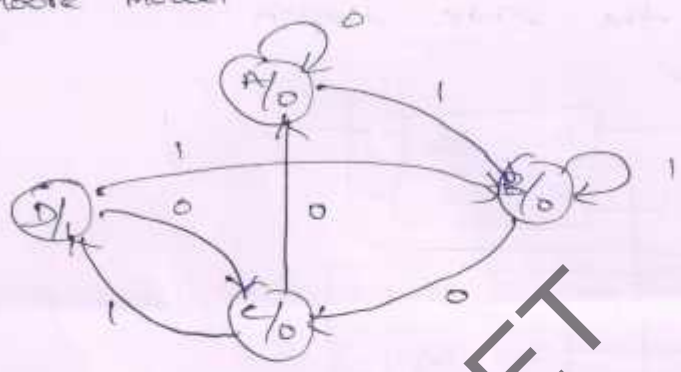
Draw the transition table.

$T_C = Q_A$ $T_B = \bar{Q}_C$ $T_A = 1$

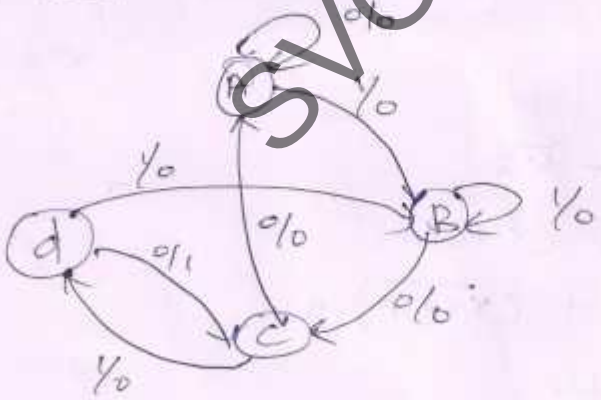


12. Draw the state transition diagram of a seq. detector ckt that detects 1010 from input data stream using moore model & mealy model

Moore model



Mealy model



Present state	Next state x=0	Next state x=1	Y x=0	Y x=1
A	A	B	0	0
B	C	B	0	0
C	A	D	0	0
D	R	B	1	0

13 A seq. ckt has two ff A & B. The ff input functions are $J_A = B$ $K_A = B\bar{x}$

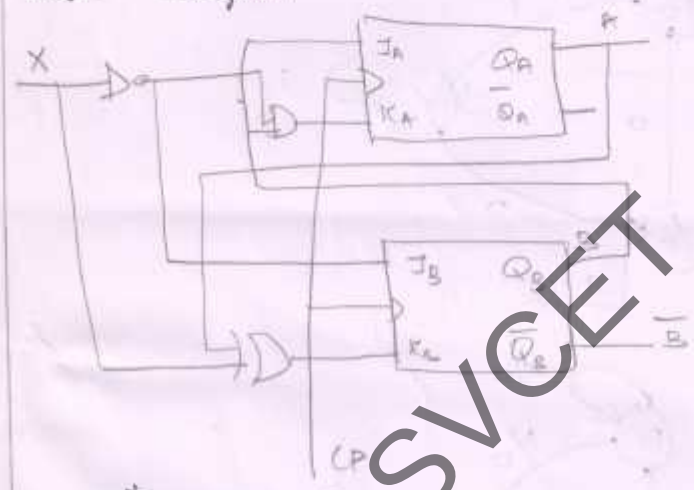
$J_B = \bar{x}$ $K_B = A \oplus x$ $F = A \oplus B$

(i) Draw the logic dia of ckt

(ii) Tabulate the state table

(iii) Draw the state diagram

Logic diagram



$Q^+ = J\bar{Q} + \bar{K}Q$

$A^+ = B\bar{A} + (x + \bar{B})A$

$B^+ = \overline{xB} + (\overline{x \oplus A}).B$

Transition table

Present state		Next state				Output
		x=0		x=1		
A	B	A^+	B^+	A^+	B^+	$F = A \oplus B$
0	0	0	1	0	0	0
0	1	1	1	1	0	1
1	0	1	1	1	0	1
1	1	0	0	1	1	0