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Subject Code/ Name: EE6301/ DIGITAL LOGIC CIRCUITS

UNIT II-COMBINATIONAL CIRCUITS

PART – A

1. Give the 2 canonical forms of Boolean function.

1. Sum of products 2. Product of sums

2. What is minterm & maxterm? A product term containing all the „n“ variables of the function in either complemented or uncomplemented form is called minterm. A sum term containing all the „n“ variables of the function in either complemented or Uncomplemented form is called maxterm.

3. What is SOP, POS?

The sum of products expression consists of two or more product (AND) terms that are OR ed together. Each product term consists of one or more literals in either complemented or Uncomplemented form.

The product of sums expression consists of two or more sum (OR) terms that are AND ed together. Each sum term consists of one or more literals in either complemented or uncomplemented form.

4. What is a K- map?

Karnaugh map is a useful tool for simplifying and manipulating switching functions. It is a map containing 2^n cells for a „n“ variable case. Each cell corresponds to one row of the truth table.

5. What is prime implicant and non-prime implicant?

Prime implicant is a product term obtained by combining the maximum possible number of adjacent squares in the K-map. It can not be enclosed by a larger implicant. Non prime implicant can be enclosed by a larger group.

6. What is essential prime implicant?

If a minterm is covered by only one prime implicant that is said to be essential and it must be included in the minimum sum of products.

7. What is incompletely specified functions/don't care conditions?

In certain digital systems some combinations of input variables do not occur. The outputs corresponding to that input combinations do not matter. So the designer can assume a 0 or 1 as output for each of these combinations. This condition is known as don't care conditions denoted by X in K-map.

8. What are the limitations of K-map?

The map method is convenient as long as the number of variables does not exceed five or six. As the number of variable increases, the excessive number of squares prevents a reasonable selection of adjacent squares.

9. What is tabulation method?

The tabulation or Quine McCluskey method is a specific step by step procedure guaranteed to produce a simplified standard form expression for a function. It can be applied to problems with many variables and has the advantage of being suitable for machine computation.

10. What is the need for a code converter?

The availability of a large variety of codes for the same discrete elements of information results in the use of different codes for different digital systems. It is sometimes necessary to use the output of one system as the input to another. A conversion circuit must be inserted between the two systems if each uses different codes for the same information. Thus a code converter is a circuit that makes the two systems compatible even though each uses a different binary code.

11. What are the steps to design a combinational logic circuit?

- (1) The problem is stated
- (2) The number of available input variables and required output variables is determined
- (3) The input and output variables are assigned letter symbols
- (4) The truth table that defines the required relationships between inputs and outputs is derived
- (5) The simplified Boolean function for each output is obtained
- (6) The logic diagram is drawn

12. What is an Encoder & Decoder?

An encoder is a combinational circuit that has 2^n input lines and „n“ output lines. The output lines generate the binary code corresponding to the input value. eg. octal to binary encoder has 8 inputs and 3 outputs that generate the binary number corresponding to the octal digit.

The decoder is a combinational circuit that converts binary information from „n“ input lines to a maximum of 2^n unique output lines. A binary code of n bits is capable of representing up to 2^n distinct elements.

13. What is a Multiplexer and Demultiplexer?

Multiplexing means transmitting a large number of information units over a smaller number of channels or lines.

A digital Multiplexer (data selector) is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. A Demultiplexer (data distributor) is a combinational circuit that receives the information on a single line and transmits this information on one of 2^n possible output lines.

14. Mention the applications of Multiplexer.

- 1) Data selection and data routing.
- 2) Logic function generator.
- 3) Control sequencer.
- 4) Parallel to serial converter.

15. Compare decoder and Demultiplexer.

The Decoder is a combinational circuit that converts binary information from „n“ input lines to a maximum of 2^n unique output lines. A Demultiplexer (data distributor) is a combinational circuit that receives the information on a single line and transmits this information on one of 2^n possible output lines. A decoder with enable input can function as a Demultiplexer.

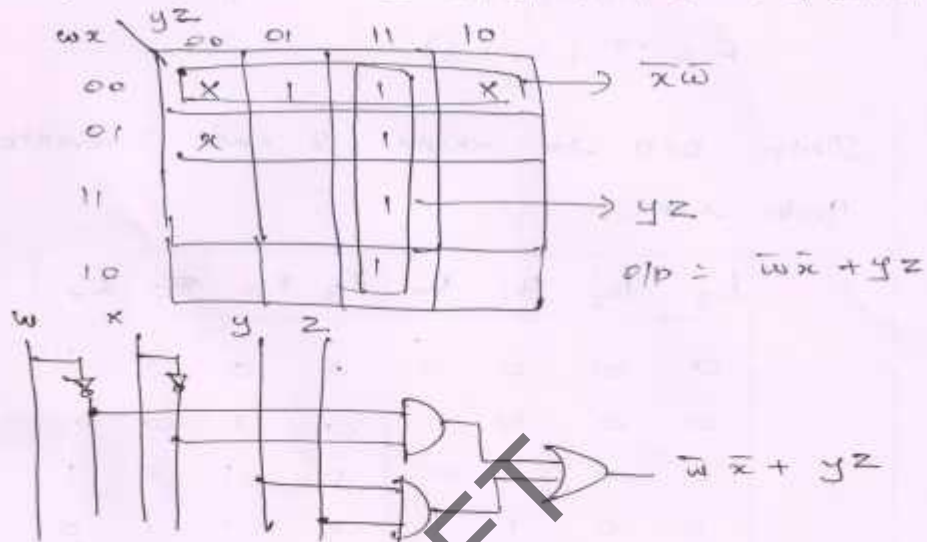
PART B

SVCET

Unit II

1. Simplify the Boolean fun using Kmap
 $F(w, x, y, z) = \sum (1, 3, 7, 11, 15)$ which are the don't care conditions
 $d(w, x, y, z) = \sum (0, 2, 5)$

Soln
 $F(w, x, y, z) = \sum (1, 3, 7, 11, 15) + d(0, 2, 5)$



Express the fun $F = A + \bar{B}$

- (a) Canonical SOP Form (b) Canonical POS Form
 (c) Canonical SOP Form

$$F = A + \bar{B}$$

$$= ABC + ABC\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C + A\bar{B}\bar{C}$$

$$= m_7 + m_6 + m_5 + m_3 + m_2 + m_1$$

$$F = \sum (1, 3, 5, 6, 7)$$

(b) POS form

$$F = A + \bar{B}C$$

$$= (A + \bar{B} + C) \cdot (A + \bar{B} + \bar{C}) \cdot (A + B + C) \cdot (A + \bar{B} + C)$$

$$= M_2 M_3 M_0$$

$$F = \prod (0, 2, 3)$$

3. Design BCD to excess 3 code converter

Truth table

B_3	B_2	B_1	B_0	E_3	E_2	E_1	E_0
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

$$E_0 = \bar{B}_0 ; \quad E_1 = B_1 \oplus B_0$$

$$E_2 = B_2 \bar{B}_1 \bar{B}_0 + \bar{B}_2 (B_0 + B_1)$$

$$E_3 = B_3 + B_2 (B_0 + B_1)$$

Draw the logic diagram.

4. Simplify the K-map.

$$F(A, B, C, D) = \sum m(7, 8, 9) + d(11, 12, 14, 13, 15, 10)$$

$$= 0111 + 1000 + 1001 + 1010 + 1011 + 1100 + 1101 + 1110 + 1111$$

$$F(A, B, C, D) = A + BCD$$

		CD			
	AB	00	01	11	10
00					
01				1	
11		X	X	X	X
10		1	1	X	X

Diagram showing K-map simplification for $F(A, B, C, D) = A + BCD$. The K-map is a 4x4 grid with rows labeled AB (00, 01, 11, 10) and columns labeled CD (00, 01, 11, 10). The function value is 1 for minterms 7, 8, 9 and don't care terms 11, 12, 14, 13, 15, 10. The simplified expression is $F(A, B, C, D) = A + BCD$. A group of four 1s in the row AB=11 is circled and labeled 'A'. A group of three 1s in the column CD=11 is circled and labeled 'BCD'.

5.

Design
Converter

2421

code to

excess 3 code

2	4	21	
A	B	C	D
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Excess 3 code

E ₃	E ₂	E ₁	E ₀
0	0	1	1
0	0	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

produce carry

$$F_2 = A + BD + BC$$

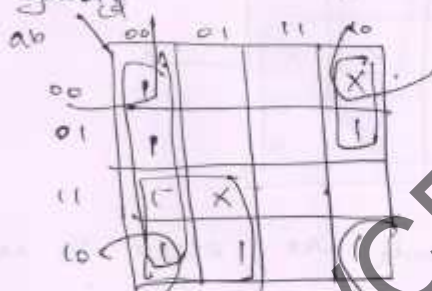
$$F_2 = B\bar{C}\bar{D} + \bar{B}D + \bar{B}C$$

$$F_1 = \bar{C}\bar{D} + CD$$

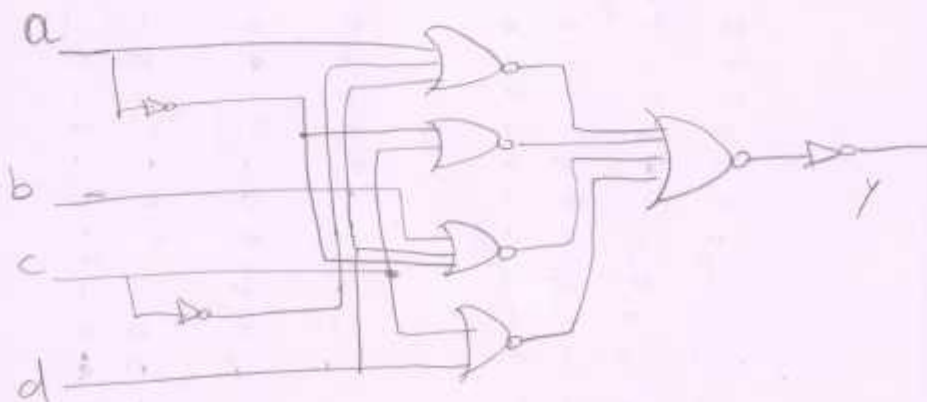
$$F_0 = \bar{D}$$

6. Minimize the function $F(a, b, c, d) = \sum (0, 4, 6, 8, 9, 10, 12)$
with $d = \sum (2, 13)$. Implement the fn using only

NOR gates



$$F(a, b, c, d) = \bar{c}\bar{d} + a\bar{c} + a\bar{b}d + \bar{a}cd$$



7. Prove that $F = \bar{A} \cdot B + A \cdot \bar{B}$ is exclusive OR operation & it equals to

$$\overline{\overline{A \cdot B} \cdot A} \cdot \overline{\overline{A \cdot B} \cdot B}$$

$$\bar{A} \cdot B + A \cdot \bar{B} = \overline{\overline{A \cdot B} \cdot A} \cdot \overline{\overline{A \cdot B} \cdot B}$$

$$\text{R.H.S} = \overline{\overline{A \cdot B} \cdot A} + \overline{\overline{A \cdot B} \cdot B}$$

$$= \bar{A} \cdot B \cdot A + \bar{A} \cdot \bar{B} \cdot B$$

$$= (\bar{A} + \bar{B}) \cdot A + (\bar{A} + \bar{B}) \cdot B$$

$$= \bar{A}A + A\bar{B} + \bar{A}B + \bar{B}B$$

$$= \bar{A}B + A\bar{B}$$

$$= \text{L.H.S}$$

8. Give the simplified expression for the following logic equation where d represents don't care condition.

$$f(A, B, C, D) = \sum m(0, 8, 11, 12, 15) + d(1, 2, 4, 7, 10, 14)$$

Represent the simplified expression using logic gates.

AB	00	01	11	10
00	1	X		X
01	X			
11	1		1	X
10	1		1	X

$$f(A, B, C, D) = \bar{C}\bar{D} + AC$$



9. Write a brief note on the following
 (i) De Morgan's theorem

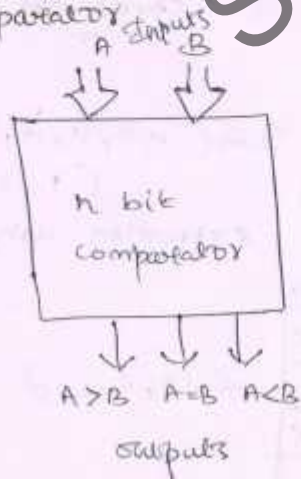
Theorem 1 : $\overline{AB} = \bar{A} + \bar{B}$

A	B	\overline{AB}	\bar{A}	\bar{B}	$\bar{A} + \bar{B}$
0	0	1	1	1	1
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	0	0	0

Theorem 2 : $\overline{A+B} = \bar{A} \cdot \bar{B}$

A	B	$A+B$	$\overline{A+B}$	\bar{A}	\bar{B}	$\bar{A} \cdot \bar{B}$
0	0	0	1	1	1	1
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	0

(ii) Comparator



(iii) Binary to Gray code converter

Gray code is non weighted code.

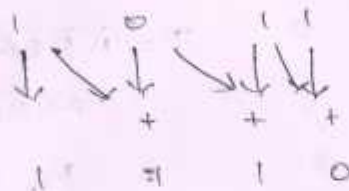
→ Record the MSB as it is

→ Add this bit to the next position.

→ recording the sum and neglecting any carry

→ Record the successive sum until completed.

MS.B



Ans : 1110

(iv) Multiplexer

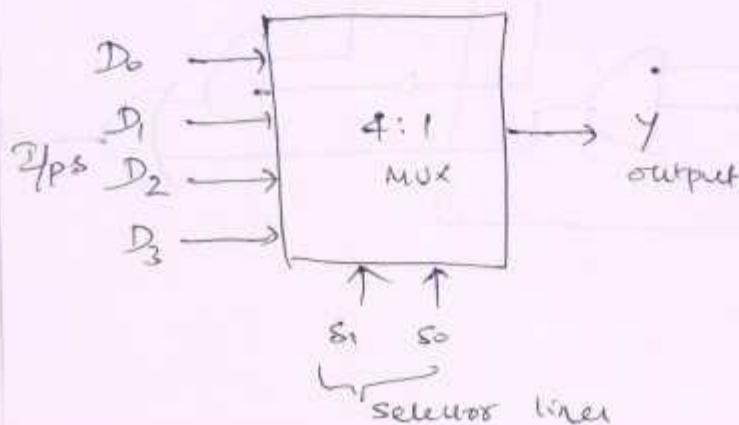
4:1 MUX

S_1	S_0	F
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

$$2^n : 1 = 2^2 : 1 = 4 : 1$$

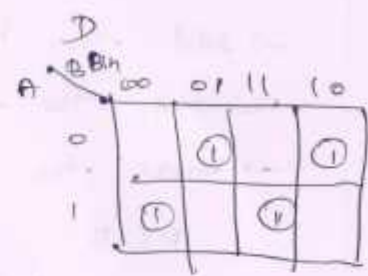
2 → input, 2 selector lines

& 1 output



10. Design a full subtractor using half subtractors and implement it using logic gates.

Inputs			Outputs	
A	B	Bin	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

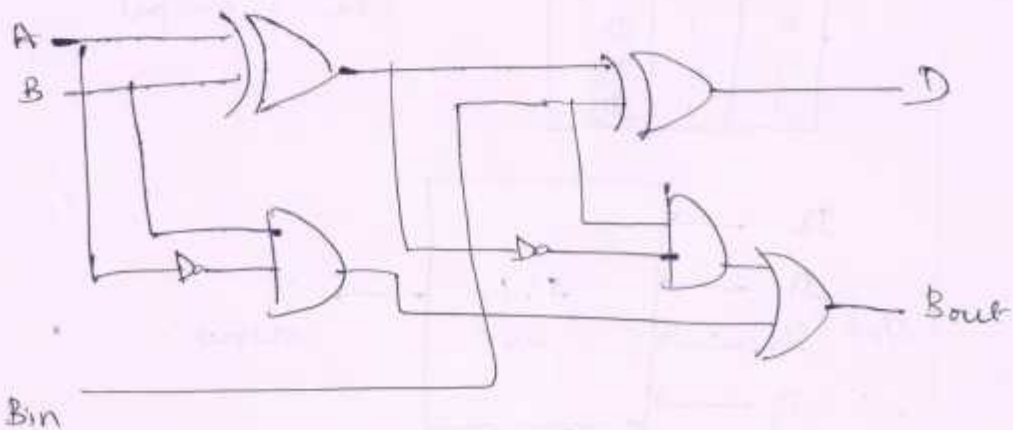


$$D = \bar{A}\bar{B}Bin + \bar{A}B\bar{B}in + A\bar{B}Bin + AB\bar{B}in$$

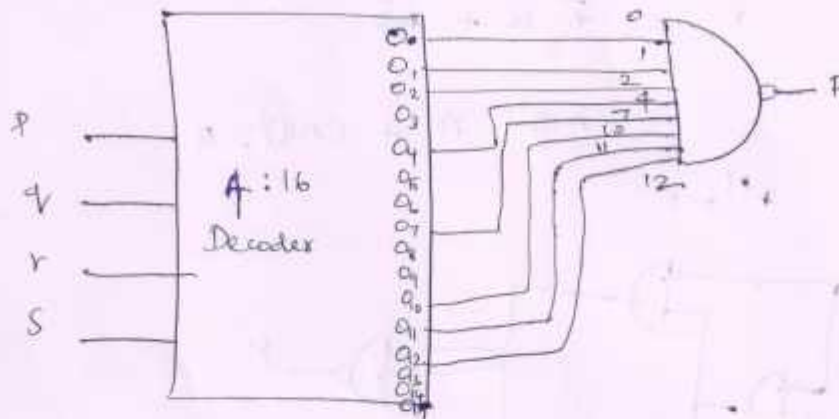
$$= Bin \oplus (A \oplus B)$$



$$Bout = \bar{A}Bin + \bar{A}B + BBin$$



11. Implement the fn $F(p, q, r, s) = \sum (0, 1, 2, 4, 7, 10, 11, 12)$ using decoder.



12. How can you convert 4 x 16 Decodes to 16x1 mux?

In 4 x 16 Decoder

S_0, S_1, S_2, S_3 are 4 inputs ;

E - Enable

16 outputs, D_0, D_1, \dots, D_{15}

16 x 1 mux

$I_0, I_1, I_2, \dots, I_{15}$ are inputs

S_0, S_1, S_2 & S_3 are selector line

one output Y

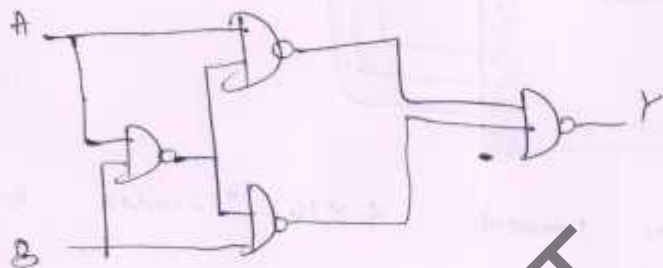
Draw the logic diagram.

13. Prove that for constructing XOR from NANDs we need four NAND gates.

$$F = \bar{A}B + A\bar{B}$$

$$= (AB)'. A + (AB)'. B$$

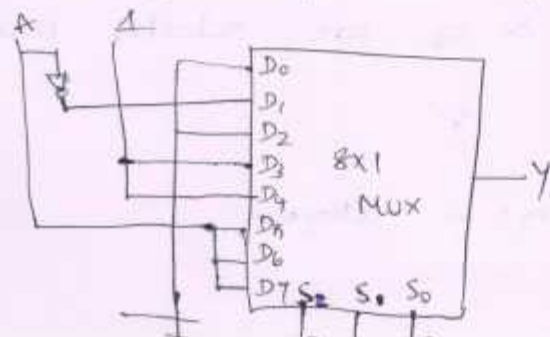
$$F'' = F$$



14. What is MUX? Implement the following Boolean fn with 8x1 MUX & external gates.

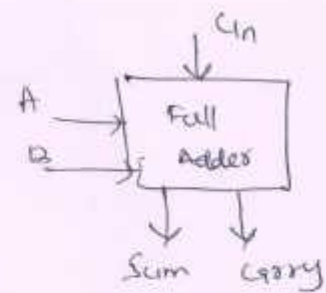
$$F(A, B, C, D) = \sum m(1, 2, 3, 4, 11, 12, 13, 14, 15)$$

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
\bar{A}	0	1	2	3	4	5	6	7
A	8	9	10	11	12	13	14	15
	0	\bar{A}	0	1	1	A	A	A



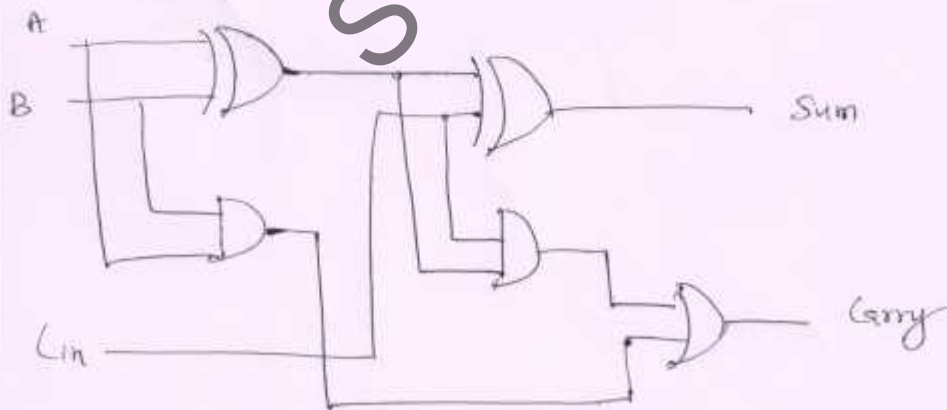
15. Design a full adder using two half adders and an OR gate.

I/p			o/p	
A	B	C _{in}	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



$$\text{Carry} = AB + AC_{in} + BC_{in}$$

$$\text{Carry Sum} = \bar{A}B C_{in} + \bar{A}B \bar{C}_{in} + A\bar{B} C_{in} + ABC_{in}$$



$$\text{Sum} = C_{in} \oplus (A \oplus B)$$