Sri Vidya College of Engineering And Technology

Virudhunagar – 626 005

Department of Electrical and Electronics Engineering

Year/ Semester/ Class : II/ III/ EEE Academic Year: 2017-2018

Subject Code/ Name: EE6301/ DIGITAL LOGIC CIRCUITS

UNIT I-NUMBER SYSTEMS & DIGITAL LOGIC FAMILIES

PART – A

1. Where the digital systems are used?

Digital systems are used extensively in computation and data processing, control systems, Communications and measurements. Since digital systems are capable of greater accuracy and reliability than analog systems, many tasks formerly done by analog are now being performed digitally.

2. What is the difference between analog and digital systems?

In a digital system the physical quantities or signals can assume only discrete values, while in analog systems the physical quantities or signals vary continuously over a specified range.

3. What is a binary number system and Why are binary numbers used in digital systems?

The number system with base (or radix) two is known as the binary number system. Only two symbols are used to represent the numbers in the system and these are 0 and 1.The outputs of the switching devices used in digital systems assume only two different values. Hence it is natural to use binary numbers internally in digital systems.

4. What is the difference between binary code and BCD?

Binary:

i. Any distinct element can be represented by a binary code.

ii. No limitation for the minimum or maximum number of elements required for coding the element.

BCD:

i. Only a decimal digit can be represented.

ii. It is a four bit representation.

5. What is an Excess3 code?

The excess3 code is a non weighted code which is obtained from the 8-4-2-1 code byadding 3(0011) to each of the codes.

6. What is a gray code and mention it‟s advantages.
A gray code is a non weighted code which has the property that the codes for successive decimal digits differ in exactly one bit.
The gray code is used in applications where the normal sequence of binary numbers may produce an error during the transition from one number to the next .

7. What is meant by non-weighted codes?
Each bit has no positional value i). Excess-3 code ii).Gray code iii).Five bit BCD

8. List the names of universal gates. Why it is named so?
NAND and NOR gates are universal gates. Because a combination of NAND gates or a combination of NOR gates can be used to perform functions of any of the basic logic gates

8. what is mean by Fanout?
Number of logic gates at the next stage that can be loaded to a given logic gate output sothat voltages for each of the possible logic state remain within the defined limits

9. What is propagation delay?
Propagation delay for a logic output from a logic gate means the time interval between change in a defined reference point input voltage and reflection of its effect at the output.
It can also be defined as the time interval between changes in a defined logic level input and reflection of its effect at the output logic level.

10. What is noise margin?
It is the maximum noise voltage added to an input signal of a digital circuit that does not cause an undesirable change in the circuit output.It is expressed in volts.

11. Explain the procedure for BCD Addition.
In BCD addition of two numbers involve following rules:-
1. Maximum value of the sum for two digits = 9 (max digit 1) + 9 (max di 1 (previous addition carry) = 19
2. If sum of two BCD digits is less than or equal to 9 (1001) without carry e result is a correct BCD number.
3. If sum of two BCD digits is greater than or equal to 10 (1010) the result is in-correct BCD number. Perform steps 4 for correct BCD sum.
4. Add 6 (0110) to the result.

12. Explain the procedure for excess 3 code.

Step 1 We have to convert the numbers (which are to be added) into excess 3 forms by adding 0011 with each of the four bit groups them or simply increasing them by 3.

Step 2 Now the two numbers are added using the basic laws of binary addition, there is no exception for this method.

Step 3 Now which of the four groups have produced a carry we have to add 0011 with them and subtract 0011 from the groups which have not produced a carry during the addition.

Step 4 The result which we have obtained after this operation is in Excess 3 form and this is our desired

13. What do you understand by self complementing code?

The 2421, the excess-3 and the 84-2-1 codes are examples of self-complementing codes. Such codes have the property that the 9's complement of a decimal number is obtained directly by changing 1's to 0's and 0's to 1's (i.e., by complementing each bit in the pattern). For example, decimal 395 is represented in the excess-3 code as 0110 1100 1000. The 9's complement of 604 is represented as 1001 0011 0111, which is obtained simply by complementing each bit of the code (as with the 1's complement of binary numbers).

14. Why the Gray code is called as reflected binary code?

The **reflected binary code** (RBC), also **known as Gray code** after Frank **Gray**, is a **binary** numeral system where two successive values differ in only one bit (**binary** digit). The **reflected binary code** was originally designed to prevent spurious output from electromechanical switches.

15. What is meant by non-weighted codes?
Each bit has no positional value i). Excess-3 code ii).Gray code iii).Five bit BCD

16. State advantages and disadvantages of TTL
Adv:

- Easily compatible with other ICs
- Low output impedance

Disadv:

- Wired output capability is possible only with tristate and open collector types
- Special circuits in Circuit layout and system design are required.
- Masked ROM.
- Programmable Read only Memory
- Erasable Programmable Read only memory.
- Electrically Erasable Programmable Read only Memory.

17. Classify the logic family by operation?
The Bipolar logic family is classified into Saturated logic, Unsaturated logic. TheRTL, DTL, TTL, I2L, HTL logic comes under the saturated logic family. The Schottky TTL, and ECL logic comes under the unsaturated logic family.

18. Mention the classification of saturated bipolar logic families.
The bipolar logic family is classified as follows:
RTL- Resistor Transistor Logic, DTL- Diode Transistor logic, I2L- Integrated Injection Logic.TTL- Transistor Transistor Logic, ECL- Emitter Coupled Logic.

19. Mention the important characteristics of digital IC‟s?
Fan out, Power dissipation, Propagation Delay, Noise Margin , Fan In, Operating temperature ,Power supply requirements.

20. What is depletion mode& enhancement mode operation MOS?
If the channel is initially doped lightly with p-type impurity a conducting channel exists at zero gate voltage and the device is said to operate in depletion mode. If the region beneath the gate is left initially uncharged the gate field must induce a channel before current can flow. Thus the gate voltage enhances the channel current and such a device is said to operate in the enhancement mode.

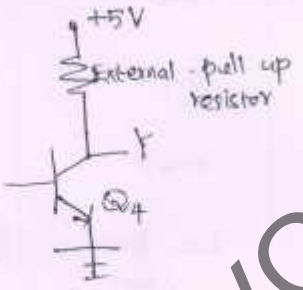
Unit I

Part B

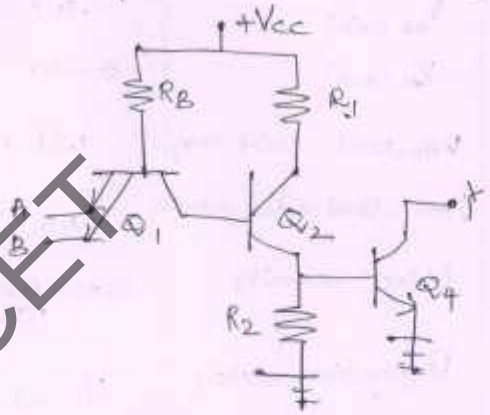
1. Explain in details about TTL with open collector output configuration.

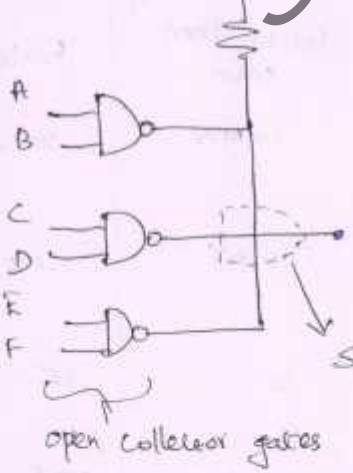
The open collector TTL gate needs an external resistor that must be connected between the collector of a pull down transistor and the supply voltage for proper operation.

Open collector o/p with external pull up resistor



Open Collector TTL NAND Gate





Disadvantage :

→ Switching delay is increased because of pull up resistance of drew kΩ.

→ The ckt is more sensitive to noise.

2. Comparision between TTL, CMOS & ECL logic families

Parameter	CMOS	TTL	ECL
Device used	N Channel & P channel MOSFET	Bipolar Jn Transistor	Bi polar Jn Transistor
V_{IH}(min)	3.5 V	2V	-1.2V
V_{IL} (max)	1.5 V	0.8V	-1.4V
V_{OH} (min)	4.95 V	2.7V	-0.9V
V_{OL} (min)	0.005V	0.4V	-1.7V
High level noise margin	1.45 V	0.4 V	0.3V
Low level noise margin	1.45 V	0.4 V	0.3V
Noise immunity	Better than TTL	Less than CMOS	More vulnerable noise
Propagation delay	70 ns	10 ns	500 ps
Switching speed	Less than TTL	Faster than CMOS	Fastest
Power dissipation per gate	0.1 MW	10 mW	25 mW
Speed power product	0.7 pJ	100 pJ	0.5 pJ
Fan out	50	10	25
Power supply voltage	3-15 V	Fixed 5V	-4.5 -5.2V
Applications	Portable instrument where battery supply is used	Lab instruments	High speed instruments

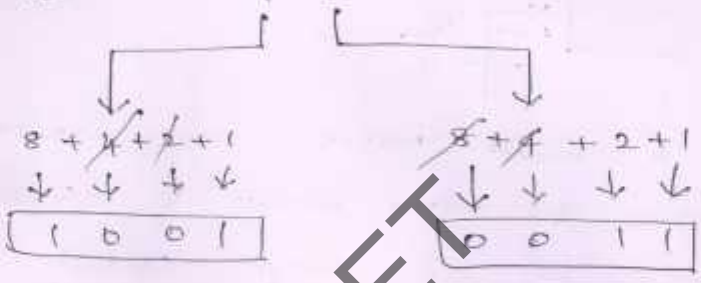
3. Briefly discuss weighted Binary code

In weighted binary code, each digit position of the no represents a specific weight.

→ Ex : 8421 code, 5421 code, 2421 code
6311 code 4221 code

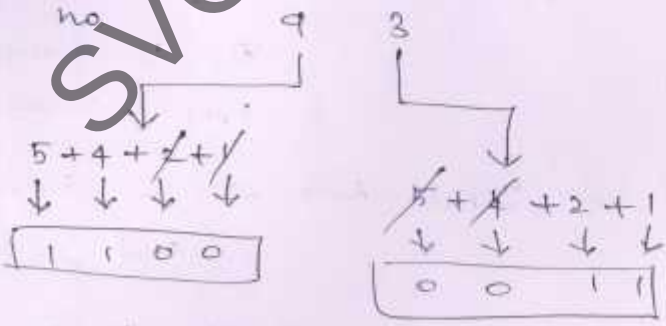
8421 code

Decimal no 9 3

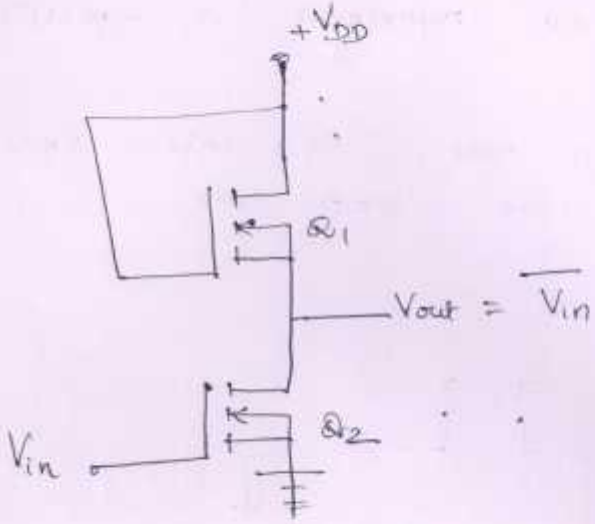


5421 code

Decimal no 9 3



4. Draw MOS logic ckt for NOT gate & explain the operation.



Two n-channel MOSFETs are connected in series. The gate of upper mosfet is connected to the drain so that it always conduct.

→ Input low → Q_2 turns off
Q_1 is always on
Output voltage is about V_{DD}

→ Input high → Q_2 turns on
Ckt behaves as an inverter

→ Resistance of Q_2 is less compared to Q_1 to maintain the output at a voltage below threshold voltage V_T.

5) Given frame with bit sequence 11010111011 is transmitted and received as 11010111010. Determine the method of detecting the error using any one error detection code.

Step 1 :

Construct a bit location table

Bit designation	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1
Bit location	10	9	8	7	6	5	4	3	2	1
Bit location numbers	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001
Received code	1	1	0	1	0	1	1	0	1	0

Step 2 : Check the parity bits

Parity check for Even is correct → 0

The resultant word is 0001.

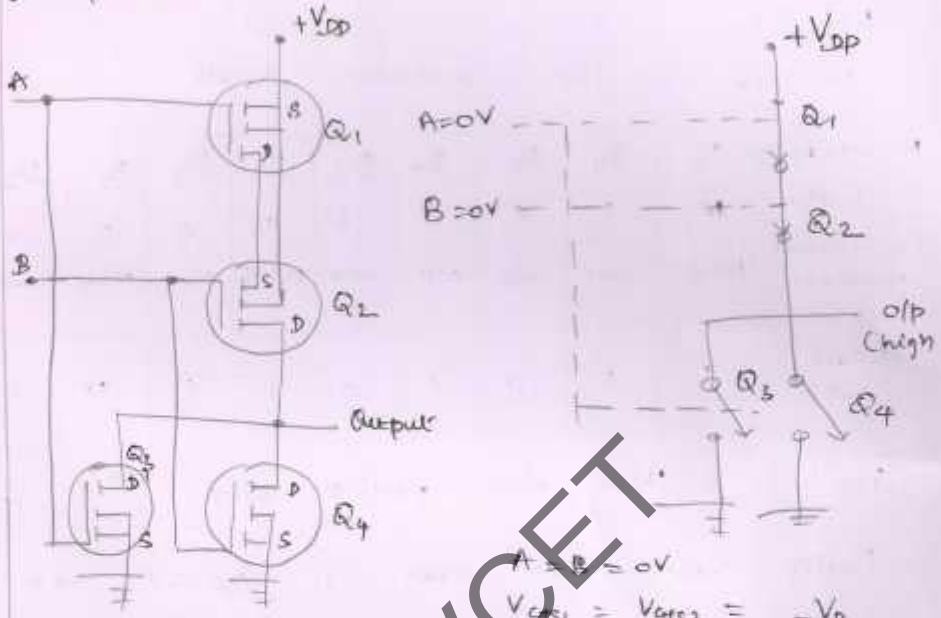
This says that the bit in the number 1 location is in error.

It is 0 & should be 1.

Therefore the correct code is 11010111011

6. Draw CMOS logic ckts for NOR gate and explain its operation.

→ P channel MOSFET Q_1 & Q_2 are connected in series and N channel MOSFETS are Q_3 & Q_4 in parallel.

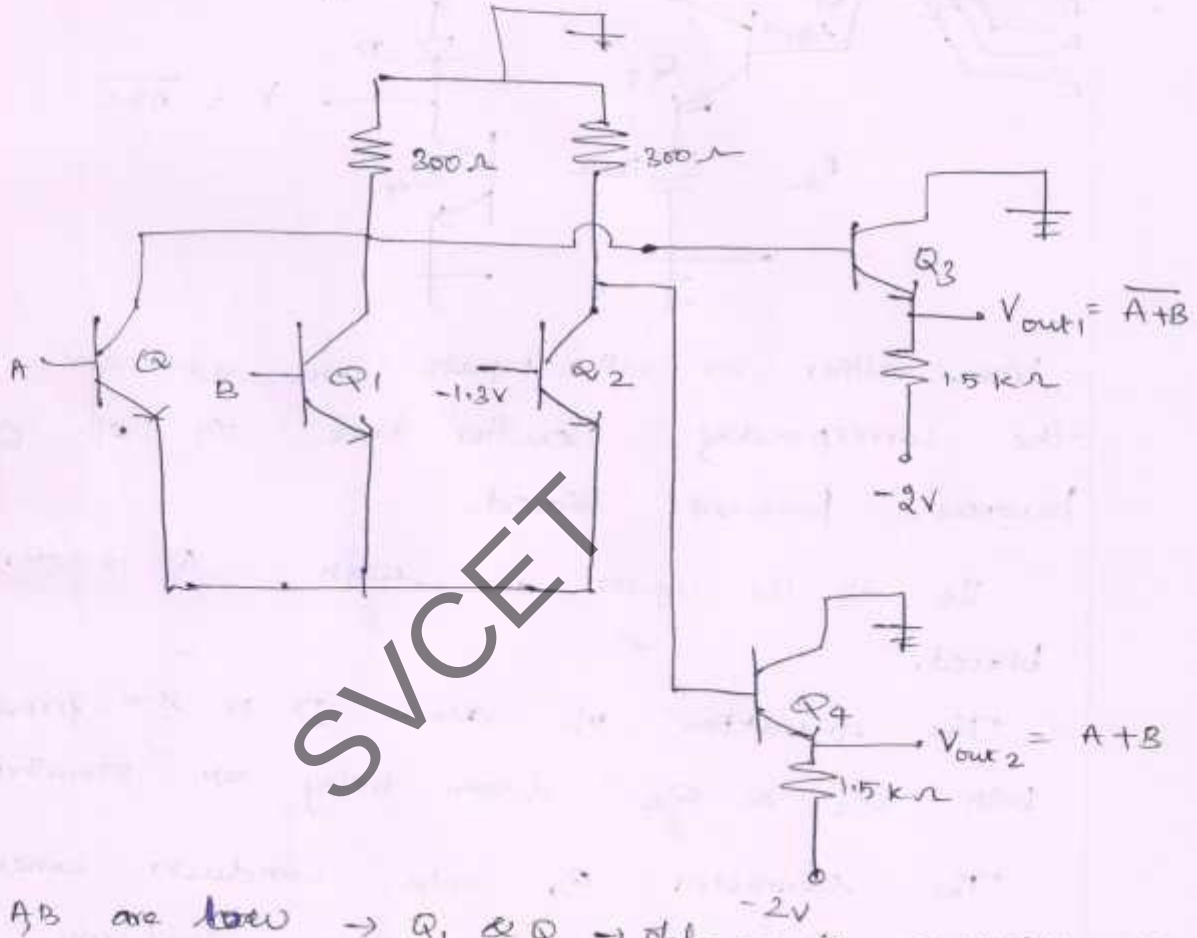


Truth table

A	B	Q_1	Q_2	Q_3	Q_4	Output
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

7. Explain the logic working principles of ECL and TTL logic families.

ECL OR/NOR logic :



A,B are low → Q_1 & Q → off → Q_2 → active region

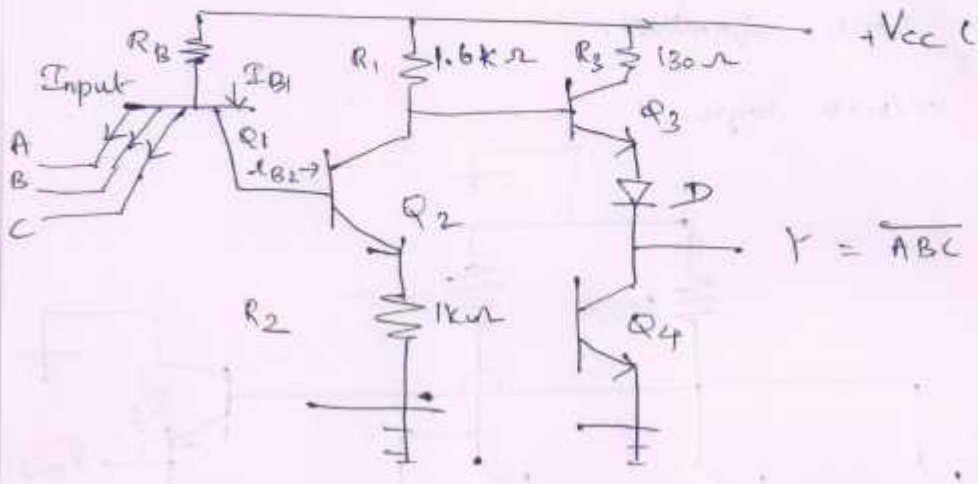
Either A or B is high → Q_2 → off

Transistor Q_3 and Q_4 provides necessary dc shift for voltage correction.

If the output is taken at V_{out1}, the ckt acts as a NOR gate

If the output is taken at V_{out2}, the ckt acts as an OR gate

8. Design TTL logic for 3 input NAND gate.



When either or all inputs are at 0V, the corresponding emitter base jn of Q_1 becomes forward biased.

If all the inputs are high, Q_1 is reverse biased.

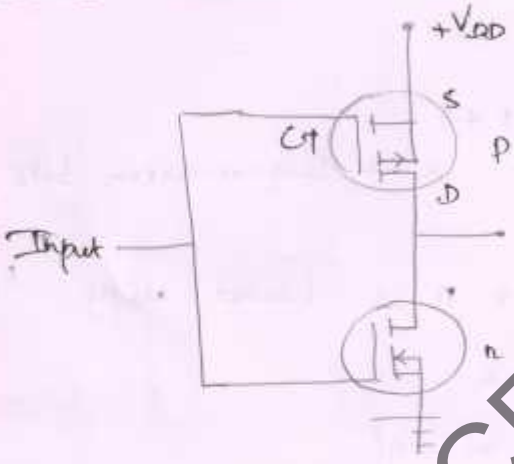
The function of diode D is to prevent both Q_3 & Q_4 from being on simultaneously.

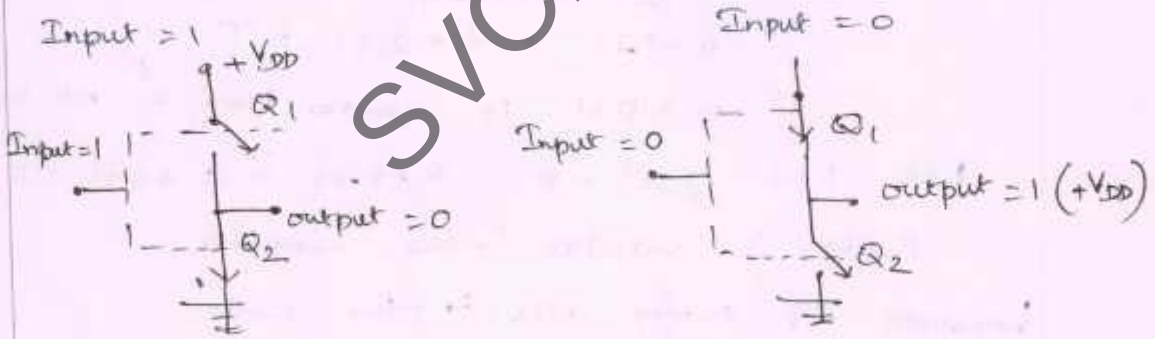
The transistor Q_4 only conducts when the output is low, which confirms the conditions for NAND operation.

9. Demonstrate the CMOS logic circuit configuration and characteristics in details.

CMOS circuit contain both NMOS and PMOS devices to speed the switching of capacitive loads.

CMOS Inverter circuit





CMOS inverter

A	Q_1	Q_2	output
0	ON	OFF	1
1	OFF	ON	0

Draw the characteristics table of CMOS

10. Explain Hamming code with an example. State its advantages over parity codes.

Hamming code is called Error detecting & correcting code.

The code uses a no of parity bits located at certain positions in the code group.

No of parity bits

$$2^p \geq x + p + 1$$

where $p \rightarrow$ parity bits $\quad x \rightarrow$ Information bits

Example:

$x = 4$ then parity p is found using trial & error method. Put $p = 2$

$2^p = 2^2 = 4$

$x + p + 1 = 4 + 2 + 1 = 7$

$x + p + 1$ is greater than 2^p not satisfied

Let $p = 3 \quad 2^3 = 8 \quad x + p + 1 = 4 + 3 + 1 = 8$

Parity 3 satisfies the condition.

Location of parity bits in the code

Bit 7, Bit 6, Bit 5, Bit 4, Bit 3, Bit 2, Bit 1

$D_7 \; D_6 \; D_5 \; D_4 \; D_3 \; D_2 \; D_1$

Assignment of P_1 : P_1 checks the location 1, 3, 5 & 7

" P_2 : P_2 checks the location of 2, 3, 6, 7

" P_4 : P_4 checks bit location of 4, 5, 6 & 7

11 Encode the binary word 1011 into seven bit even parity hamming code.

Step 1 : Find the no of parity required

Let $p = 3$ then $2^p = 2^3 = 8$

$x + p + 1 = 4 + 3 + 1 = 7$

Step 2 : Construct a bit location table

Bit designation	D_7	D_6	D_5	D_4	D_3	D_2	D_1
Bit location	7	6	5	4	3	2	1
Binary location no	111	110	101	100	011	010	001
Information bit	1	0	1		1		
Parity bit				0		0	1

Step 3 : Determine the parity bits

Step 4 : Enter the parity bits into the table to form seven hamming code

$= 1\ 0\ 1\ \underset{\leftarrow}{0}\ 1\ \underline{0\ 1}$