Year/sem: 02/04 **Academic Year: 2014-2015 (even)**

UNIT III

I/O INTERFACING

1. What is interfacing?

An interface is a shared boundary between the devices which involves sharing information. Interfacing is the process of making two different systems communicates with each other.

2. What is memory mapping?

The assignment of memory addresses to various registers in a memory chip is called as memory mapping.

3. What is I/O mapping?

The assignment of addresses to various I/O devices in the memory chip is called as I/O mapping.

4. What is an USART?

USART stands for universal synchronous/Asynchronous Receiver/ Transmitter. It is a programmable communication interface that can communicate by using either synchronous or asynchronous serial data.

5. What is the use of 8251 chip?

8251 chip is mainly used as the asynchronous serial interface between the processor and the external equipment.

6. The 8279 is a programmable _____ interface.

Keyboard/Display

7. List the major components of the keyboard/Display interface.

a. Keyboard section
b. Scan section
c. Display section
d. CPU interface section

8. What is Key bouncing?

Mechanical switches are used as keys in most of the keyboards. When a key is pressed the contact bounce back and forth and settle down only after a small time delay (about 20ms). Even though a key is actuated once, it will appear to have been actuated several times. This problem is called Key Bouncing.

9. Define HRQ?

The hold request output requests the access of the system bus. In non- cascaded 8257 systems, this is connected with HOLD pin of CPU. In cascade mode, this pin of a slave is connected with a DRQ input line of the master 8257, while that of the master is connected with HOLD input of the CPU.

10. What is the use of stepper motor?

A stepper motor is a device used to obtain an accurate position control of rotating shafts. A stepper motor employs rotation of its shaft in terms of steps, rather than continuous rotation as in case of AC or DC motor.

11. What is TXD?

TXD- Transmitter Data Output
This output pin carries serial stream of the transmitted data bits along with other information like start bit, stop bits and priority bit.

12. What is RXD?

RXD- Receive Data Input
This input pin of 8251A receives a composite stream of the data to be received by 8251A.

13. Draw the status word format for 8254.

OUT
NULL
COUNT
RW1 RW0 M2 M1 M0 BCD

14. What is meant by key bouncing?

Microprocessor must wait until the key reach to a steady state; this is known as Key bounce.

15.Write the function of crossbar switch?

The crossbar switch provides the inter connection paths between the memory module and the processor. Each node of the crossbar represents a bus switch. All these nodes may be controlled by one of these processors or by a separate one altogether.

16. What is a data amplifier?

Transceivers are the bi-directional buffers are sometimes they are called as data amplifiers. They are required to separate the valid data from the time multiplexed address data signal. They are controlled by 2 signals i.e DEN & DT/R.

17. What are the different inter connection topologies?

• Shared bus
• Multiport Memory
• Linked Input/ Output
• Bus window
• Crossbar Switching.

18. What are the configurations used for physical interconnections?

• Star Configuration
• Loop configuration
• Complete interconnection
• Regular topologies
• Irregular topologies

19. What are the functional types used in control words of 8251a?

The control words of 8251A are divided into two functional types.
1. Mode Instruction control word
2. Command Instruction control word

Mode Instruction control word:-This defines the general operational characteristics of 8251A.

Command Instruction control word:-The command instruction controls the actual operations of the selected format like enable transmit/receive, error reset and modem control.

20. What are the basic modes of operation of 8255?

There are two basic modes of operation of 8255, viz.
1. I/O mode.
3. BSR mode.

In I/O mode, the 8255 ports work as programmable I/O ports, while In BSR mode only port C (PC0-PC7) can be used to set or reset its individual port bits. Under the IO mode of operation, further there are three modes of operation of 8255, So as to support different types of applications, viz. mode 0, mode 1 and mode 2.

Mode 0 - Basic I/O mode
Mode 1 - Strobed I/O mode
Mode 2 - Strobed bi-directional I/O

21. Write the features of mode 0 in 8255?

1. Two 8-bit ports (port A and port B) and two 4-bit ports (port C upper and lower) are available. The two 4-bit ports can be combined used as a third 8-bit port.
2. Any port can be used as an input or output port.
3. Output ports are latched. Input ports are not latched.
4. A maximum of four ports are available so that overall 16 I/O configurations are possible.

22. What are the features used mode 1 in 8255?

Two groups – group A and group B are available for strobed data transfer.
1. Each group contains one 8-bit data I/O port and one 4-bit control/data port.
2. The 8-bit data port can be either used as input or output port. The inputs and outputs both are latched.

3. Out of 8-bit port C, PC0-PC2 is used to generate control signals for port B and PC3=PC5 are used to generate control signals for port A. The lines PC6, PC7 may be used as independent data lines.

23. What are the signals used in input control signal & output control signal?

Input control signal
STB (Strobe input)
IBF (Input buffer full)
INTR (Interrupt request)
Output control signal
OBF (Output buffer full)
ACK (Acknowledge input)
INTR (Interrupt request)

24. What are the features used mode 2 in 8255?

The single 8-bit port in-group A is available.
1. The 8-bit port is bi-directional and additionally a 5-bit control port is available.
2. Three I/O lines are available at port C, viz PC2-PC0.
3. Inputs and outputs are both latched.
4. The 5-bit control port C (PC3=PC7) is used for generating/accepting handshake signals for the 8-bit data transfer on port A.

25. What are the modes of operations used in 8253?

Each of the three counters of 8253 can be operated in one of the following six modes of operation.
1. Mode 0 (Interrupt on terminal count)
2. Mode 1 (Programmable monoshot)
3. Mode 2 (Rate generator)
4. Mode 3 (Square wave generator)
5. Mode 4 (Software triggered strobe)
6. Mode 5 (Hardware triggered strobe)

26. What are the different types of write operations used in 8253?

There are two types of write operations in 8253
(1) Writing a control word register
(2) Writing a count value into a count register
The control word register accepts data from the data buffer and initializes the counters, as required. The control word register contents are used for
(a) Initializing the operating modes (mode 0-mode4)
(b) Selection of counters (counter 0- counter 2)
(c) Choosing binary /BCD counters
(d) Loading of the counter registers.
The mode control register is a write only register and the CPU cannot read its contents.

27. Give the different types of command words used in 8259a?

The command words of 8259A are classified in two groups
1. Initialization command words (ICWs)
2. Operation command words (OCWs)

28. Give the operating modes of 8259a?

(a) Fully Nested Mode
(b) End of Interrupt (EOI)
(c) Automatic Rotation
(d) Automatic EOI Mode
(e) Specific Rotation
(f) Special Mask Mode
(g) Edge and level Triggered Mode

(h) Reading 8259 Status
(i) Poll command
(j) Special Fully Nested Mode
(k) Buffered mode
(l) Cascade mode

29. Define scan counter?

The scan counter has two modes to scan the key matrix and refresh the display. In the encoded mode, the counter provides binary count that is to be externally decoded to provide the scan lines for keyboard and display. In the decoded scan mode, the counter internally decodes the least significant 2 bits and provides a decoded 1 out of 4 scan on SL0-SL3.The keyboard and display both are in the same mode at a time.

30. What is the output modes used in 8279?

8279 provides two output modes for selecting the display options.

1. Display Scan

In this mode, 8279 provides 8 or 16 character-multiplexed displays those can be organized as dual 4-bit or single 8-bit display units.

2. Display Entry

8279 allows options for data entry on the displays. The display data is entered for display from the right side or from the left side.

31. What are the modes used in keyboard modes?

1. Scanned Keyboard mode with 2 Key Lockout.
2. Scanned Keyboard with N-key Rollover.
3. Scanned Keyboard special Error Mode.
4. Sensor Matrix Mode.

32. What are the modes used in display modes?

1. Left Entry mode

In the left entry mode, the data is entered from the left side of the display unit..

2. Right Entry Mode

In the right entry mode, the first entry to be displayed is entered on the rightmost display.

33.What is the use of modem control unit in 8251?

The modem control unit handles the modem handshake signals to coordinate the communication between the modem and the USART.

34. Give the register organization of 8257?

The 8257 perform the DMA operation over four independent DMA channels. Each of the four channels of 8257 has a pair of two 16-bit registers. DMA address register and terminal count register. Also, there are two common registers for all the channels; namely, mode set registers and status register. Thus there are a total of ten registers. The CPU selects one of these ten registers using address lines A0-A3.

35. What is the function of DMA address register?

Each DMA channel has one DMA address register. The function of this register is to store the address of the starting memory location, which will be accessed by the DMA channel. Thus the starting address of the memory block that will be accessed by the device is first loaded in the DMA address register of the channel. Naturally, the device that wants to transfer data over a DMA channel, will access the block of memory with the starting address stored in the DMA Address Register.

36. What is the use of terminal count register?

Each of the four DMA channels of 8257 has one terminal count register. This 16-bit register is used for ascertaining that the data transfer through a DMA channel ceases or stops after the required number of DMA cycles.

37. What is the function of mode set register in 8257?

The mode set register is used for programming the 8257 as per the requirements of the system. The function of the mode set register is to enable the DMA channels individually and also to set the various modes of operation.

38. Define D/A and A/D interface

The analog to digital converter is treated as an input device by the microprocessor that sends an initializing signal to the **ADC** to start the analog to digital data conversion process.

The Digital to Analog Converters (**DAC**) convert binary numbers into their analog equivalent voltages.

39. List the applications of D/A interface

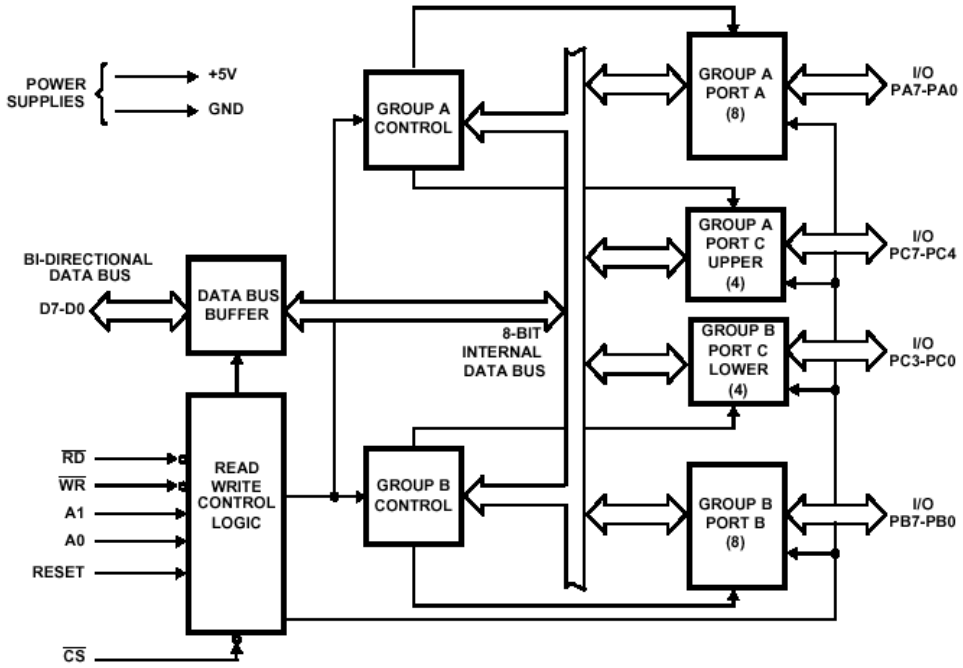
The DAC find applications in areas like Digitally controlled gains Motor speed controls Programmable gain amplifiers etc.

40. Give the applications of I/O interface

1. Traffic Light Control
2. LED and LCD Display
3. Alarm Controller

PART-B

1. With a neat block diagram, explain in detail the internal architecture of 8255 and its registers



Block Diagram of the 8255 Programmable Peripheral Interface (PPI)

Data Bus Buffer

This three-state bi-directional 8-bit buffer is used to interface the 8255 to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status informa-tion are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

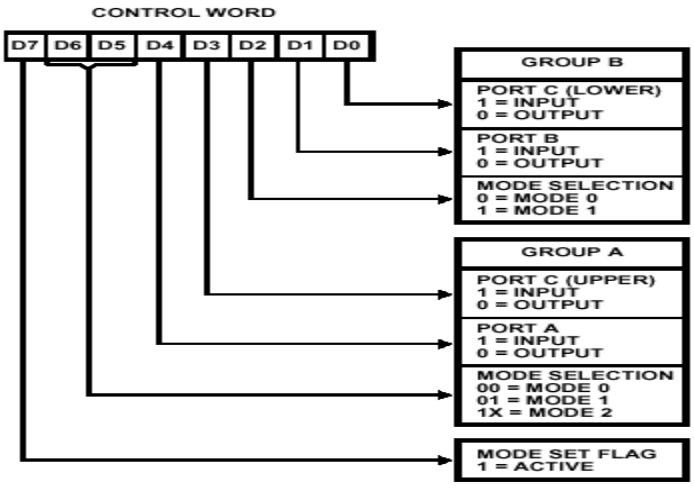
(CS) Chip Select. A "low" on this input pin enables the communcation between the 8255 and the CPU.

(RD) Read. A "low" on this input pin enables 8255 to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255.

(WR) Write. A "low" on this input pin enables the CPU to write data or control words into the 8255.
(A0 and A1) Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word register. They are normally connected to the least significant bits of the address bus (A0 and A1).
(RESET) Reset. A "high" on this input initializes the control register to 9Bh and all ports (A, B, C) are set to the input mode.

A1	A0	SELECTION
0	0	PORT A
0	1	PORT B
1	0	PORT C
1	1	CONTROL

Group A and Group B Controls
The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 8255. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 8255. Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.
Ports A, B, and C
The 8255 contains three 8-bit ports (A, B, and C). All can be configured to a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255.
Port A One 8-bit data output latch/buffer and one 8-bit data input latch. Both "pull-up" and "pull-down" bus-hold devices are present on Port A.
Port B One 8-bit data input/output latch/buffer and one 8-bit data input buffer.
Port C One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal output and status signal inputs in conjunction with ports A and B.



Mode Definition Format

2. Discuss how memory chips and I/O devices are interfaced to a microprocessor.
   Two interfaces are available
   1. Parallel Communication Interface
   2. Serial Communication Interface

Parallel Communication Interface

The **Intel 8255** (or **i8255**) Programmable Peripheral Interface chip is a peripheral chip originally developed for the Intel 8085 microprocessor, and as such is a member of a large array of such chips, known as the **MCS-85 Family**.

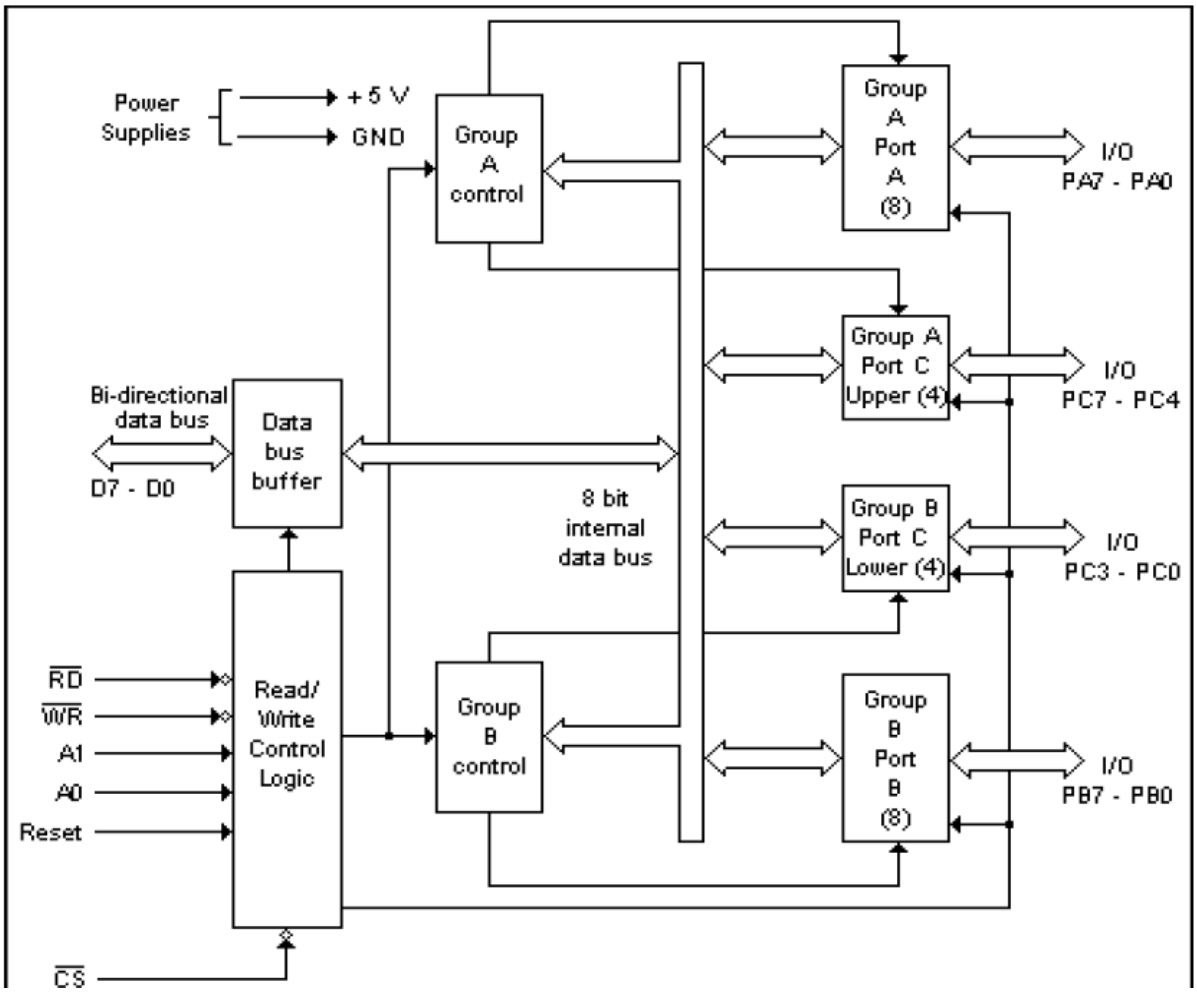
Functional Block diagram:

The 8255 has 24 input/output pins in all. These are divided into three 8-bit ports. Port A and port B can be used as 8-bit input/output ports. Port C can be used as an 8-bit input/output port or as two 4-bit input/ouput ports or to produce handshake signals for ports A and B.

The three ports are further grouped as follows:

1) Group A consisting of port A and upper part of port C.

3. 2) Group B consisting of port B and lower part of port C.



4.
5.
6.
7.

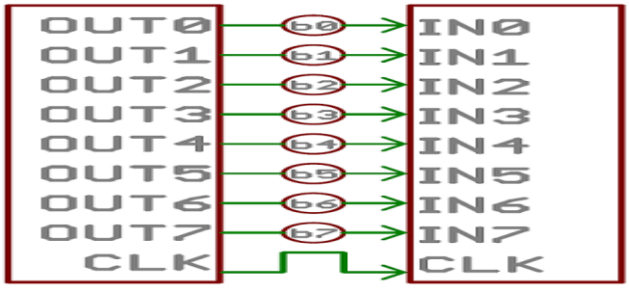
8. The control signal "' *CS"* ***(pin 6) is used to enable the 8255 chip. It is an active low signal, ie, when* CS = '0**, the 8255 is enabled. The **RESET** input (pin 35) is connected to a system (like

9. 8085, 8086, etc.) reset line so that when the system is reset, all the ports are initialised as input lines.

Serial Communication Interface.

Serial interfaces stream their data, one single bit at a time. These interfaces can operate on as little as one wire, usually never more than four.

The SCI contains a parallel-to-serial converter that serves as a data transmitter, and a serial-to-parallel converter that serves as a data receiver. The two devices are clocked separately, and use independent enable and interrupt signals. The SCI operates in a nonreturn-to-zero (NRZ) format, and can function in half-duplex mode (using only the receiver or only the transmitter) or in full duplex (using the receiver and the transmitter simultaneously). The data speed is programmable.



Asynchronous Serial

Over the years, dozens of serial protocols have been crafted to meet particular needs of embedded systems. USB (universal *serial* bus), and Ethernet, are a couple of the more well-known computing serial interfaces. Other very common serial interfaces include SPI, I^2C, and the serial standard we're here to talk about today. Each of these serial interfaces can be sorted into one of two groups: synchronous or asynchronous.

A synchronous serial interface always pairs its data line(s) with a clock signal, so all devices on a synchronous serial bus share a common clock. This makes for a more straightforward, often faster serial transfer, but it also requires at least one extra wire between communicating devices. Examples of synchronous interfaces include SPI, and I^2C.

Rules of Serial

The asynchronous serial protocol has a number of built-in rules - mechanisms that help ensure robust and error-free data transfers. These mechanisms, which we get for eschewing the external clock signal, are:

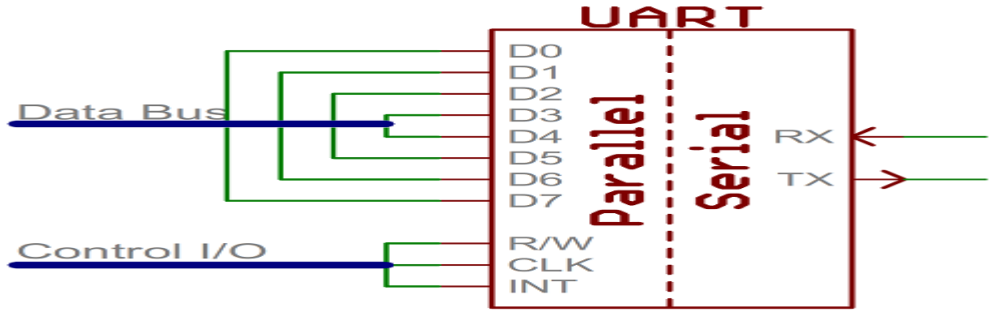
- Data bits,
- Synchronization bits,
- Parity bits,
- and Baud rate.

Through the variety of these signaling mechanisms, you'll find that there's no one way to send data serially. The protocol is highly configurable. The critical part is making sure that **both devices on a serial bus are configured to use the exact same protocols**.

UARTs

The final piece to this serial puzzle is finding something to both create the serial packets and control those physical hardware lines. Enter the UART.

A universal asynchronous receiver/transmitter (UART) is a block of circuitry responsible for implementing serial communication. Essentially, the UART acts as an intermediary between parallel and serial interfaces. On one end of the UART is a bus of eight-or-so data lines (plus some control pins), on the other is the two serial wires - RX and TX.



10. Explain the block diagram of the 8279 Keyboard/Display interface and its operations.

8279 Programmable Keyboard/Display Controller and Interfacing

The Keyboard/Display Controller 8279

Intel's 8279 is a general purpose Keyboard Display controller that simultaneously drives the display of a system and interfaces a Keyboard with the CPU. The Keyboard Display interface scans the Keyboard to identify if any key has been pressed and sends the code of the pressed key to the CPU. It also transmits the data received from the CPU.

Both of these functions are performed by the controller in repetitive fashion without involving the CPU. The Keyboard is interfaced either in the interrupt or the polled mode. In the interrupt mode, the processor is requested service only if any key is pressed, otherwise the CPU can proceed with its main task.

In the polled mode, the CPU periodically reads an internal flag of 8279 to check for a key pressure. The Keyboard section can interface an array of a maximum of 64 keys with the CPU. The Keyboard entries (key codes) are debounced and stored in an 8-byte FIFO RAM that is further accessed by the CPU to read the key codes. If more than eight characters are entered in the FIFO (i.e. more that eight keys are pressed), before any FIFO read operation, the overrun status is set. If a FIFO contains a valid key entry, the CPU is interrupted (in interrupt mode) or the CPU checks the status (in polling) to read the entry.

Once the CPU reads a key entry, the FIFO is updated, i.e. the key entry is pushed out of the FIFO to generate space for new entries. The 8279 normally provides a maximum of sixteen 7-seg display interface with CPU It contains a 16-byte display RAM that can be used either as an integrated block of 16x8-bits or two 16x4-bit block of RAM. The data entry to RAM block is controlled by CPU using the command words of the 8279.

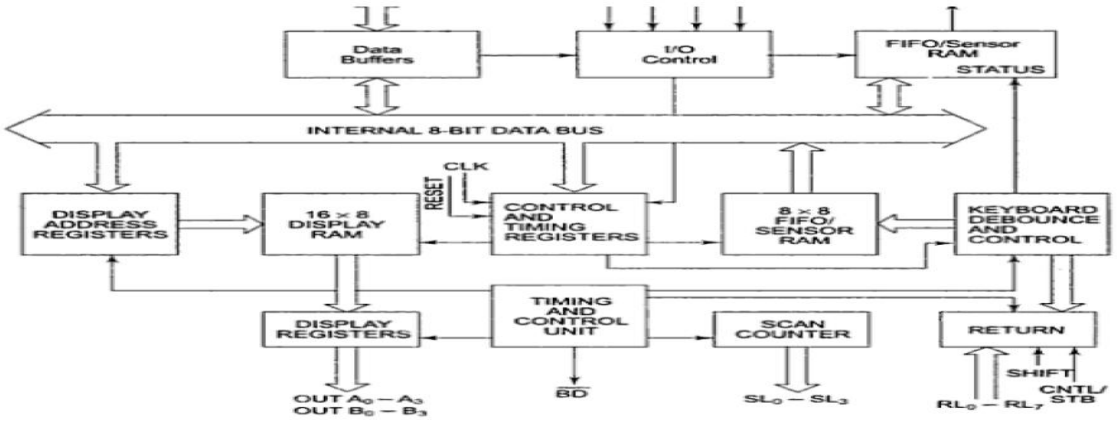
Architecture and Signal Descriptions of 8279

The Keyboard display controller chip 8279 provides
1. A set of four scan lines and eight return lines for interfacing keyboards.
2. A set of eight output lines for interfacing display.

I/O Control and Data Buffer

The I/O control section controls the flow of data to/from the 8279. The data buffer interface the external bus of the system with internal bus of 8279. the I/O section is enabled only if D is low.

8279 Internal Architecture



The pin Ao, RD and WR select the command, status or data read/write operations carried out by the CPU with 8279.

Control and Timing Register and Timing Control

These registers store the keyboard and display modes and other operating conditions programmed by CPU. The registers are written with Ao=1 and WR =0. The timing and control unit controls the basic timings for the operation of the circuit. Scan Counter divide down the operating frequency of 8279 to derive scan keyboard and scan display frequencies.

Scan Counter

The Scan Counter has two modes to scan the key matrix and refresh the display.In the Encoded mode, the counter provides a binary count that is to be externally decoded to provide the scan lines for keyboard and display (four externally decoded scan lines may drive up to 16 displays).

In the decoded scan mode, the counter internally decodes the least significant 2 bits and provides a decoded 1 out of 4 scan on SL0-SL3 (four internally decoded scan lines may drive up to 4 Displays). The Keyboard and Display both are in the same mode at a time.

Return Buffers and Keyboard Debounce and Control

This section scans for a Key closure row-wise. If it is detected, the Keyboard debounce unit debounces the key entry (i.e. wait for 10 ms). After the debounce period, if the key continues to be detected. The code of the Key is directly transferred to the sensor RAM along with SHIFT and CONTROL key status.

FIFO/Sensor RAM and Status Logic

In Keyboard or strobed input mode, this block acts as 8-byte first-in-first-out (FIFO) RAM. Each key code of the pressed key is entered in the order of the entry, and in the meantime, read by the CPU, till the RAM becomes empty. The status logic generates an interrupt request after each FIFO read operation till the FIFO is empty.

In scanned sensor matrix mode, this unit acts as sensor RAM. Each row of the sensor RAM is loaded with the status of the corresponding row of sensors in the matrix. If a sensor changes its state, the IRQ line goes high to interrupt the CPU.

Display Address Registers and Display RAM.

The Display address registers hold the addresses of the word currently being written or read by the CPU to or from the display RAM. The contents of the registers are automatically updated by 8279 to accept the next data entry by CPU. The 16-byte display RAM contains the 16-byte of data to be displayed on the sixteen 7-seg displays in the encoded scan mode.

6. What is Interrupt? Explain enabling, disabling and masking of interrupts with examples. How to transfer data using interrupts.

Interrupt is a mechanism by which an I/O or an instruction can suspend the normal execution of processor and get itself serviced. Generally, a particular task is assigned to that interrupt signal. In the microprocessor based system the interrupts are used for data transfer between the peripheral devices and the microprocessor.

Interrupt Service Routine(ISR)

A small program or a routine that when executed services the corresponding interrupting source is called as an ISR.

Maskable/Non-Maskable Interrupt

An interrupt that can be disabled by writing some instruction is known as Maskable Interrupt otherwise it is called Non-Maskable Interrupt.

There are 6 pins available in 8085 for interrupt:

1. TRAP
2. RST 7.5
3. RST6.5
4. RST5.5
5. INTR
6. INTA

Execution of Interrupts

When there is an interrupt requests to the Microprocessor then after accepting the interrupts Microprocessor send the INTA (active low) signal to the peripheral. The vectored address of particular interrupt is stored in program counter. The processor executes an interrupt service routine (ISR) addressed in program counter.

There are two types of interrupts used in 8085 Microprocessor:

1. Hardware Interrupts
2. Software Interrupts

Software Interrupts

A software interrupts is a particular instructions that can be inserted into the desired location in the rpogram. There are eight Software interrupts in 8085 Microprocessor. From RST0 to RST7.

1. RST0
2. RST1
3. RST2
4. RST3
5. RST4
6. RST5
7. RST6
8. RST7

They allow the microprocessor to transfer program control from the main program to the subroutine program. After completing the subroutine program, the program control returns back to the main program.

We can calculate the vector address of these interrupts using the formula given below:

Vector Address = Interrupt Number * 8

For Example:

RST2: vector address=2*8 = 16

RST1: vector address=1*8 = 08

RST3: vector address=3*8 = 24

Vector address table for the software interrupts:

Interrupt	**Vector Address**
RST0 RST1	0000_H 0008_H
RST2 RST3	0010_H 0018_H

RST4 RST5	0020_H 0028_H
RST6 RST7	0030_H 0038_H

Hardware Interrupt

As i have already discussed that there are 6 interrupt pins in the microprocessor used as Hardware Interrupts given below:

1. TRAP
2. RST7.5
3. RST6.5
4. RST5.5
5. INTR

7. Explain how the 8237 DMA controller transfers 64K bytes of data per channel with eight address lines.

DMA

Direct Memory Access and DMA-controlled I/O Introduction: In this chapter, we provide examples and a detailed explanation of the DMA I/O technique used in personal computer systems including those using Intel family of microprocessors.

Basic DMA operation

The direct memory access (DMA) I/O technique provides direct access to the memory while the microprocessor is temporarily disabled.

• A DMA controller temporarily borrows the address bus, data bus, and control bus from the microprocessor and transfers the data bytes directly between an I/O port and a series of memory locations.

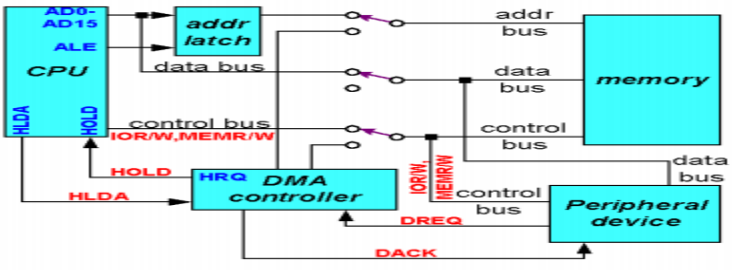
• The DMA transfer is also used to do high-speed memory-tomemory transfers.

• Two control signals are used to request and acknowledge a DMA transfer in the microprocessor-based system.

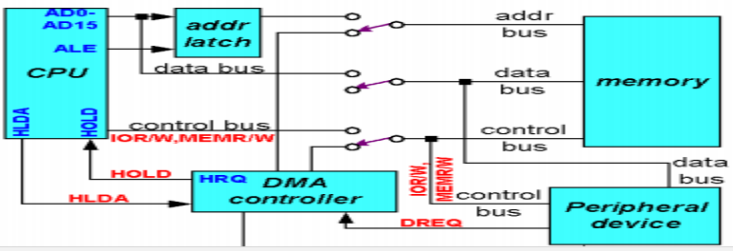
• The HOLD signal is a bus request signal which asks the microprocessor to release control of the buses after the current bus cycle.

• The HLDA signal is a bus grant signal which indicates that the microprocessor has indeed released control of its buses by placing the buses at their high-impedance states.

• The HOLD input has a higher priority than the INTR or NMI interrupt inputs

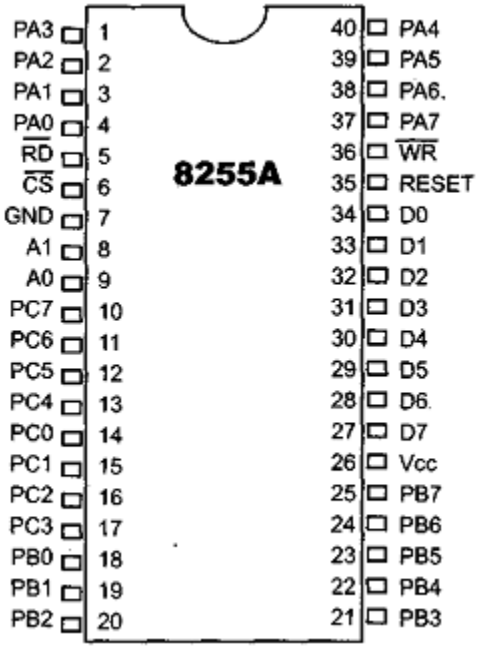


When DMA does not operate



8. Specify handshaking signals and their functions if port A of 8255 is set-up as input port in mode 1.

The 8255 is programmed as a simple I/O port for connection with devices such as LCDs, stepper motors, and ADCs



8. .Explain mode 0 and mode 1 of 8253.

The 8253/54 solves one of most common problem in any microcomputer system, the generation of accurate time delays under software control.

The 8253/54 includes three identical 16 bit counters that can operate independently. To operate a counter, a 16-bit count is loaded in its register and, on command, it begins to decrement the count until it reaches 0. At the end of the count, it generates a pulse that can be used to interrupt the CPU. The counter can count either in binary or BCD. In addition, a count can be read by the CPU while the counter is decrementing. In this chapter, we are going to study two timer ICs 8253 and 8254. The 8254 is a superset of 8253.

The functioning of these two ICs are almost similar along with the pin configuration. Only the differences are:

Features

Three independent 16-bit down counters.

8254 can handle inputs from DC to 10 MHz (5MHz 8254-5 8MHz 8254

10MHz 8254-

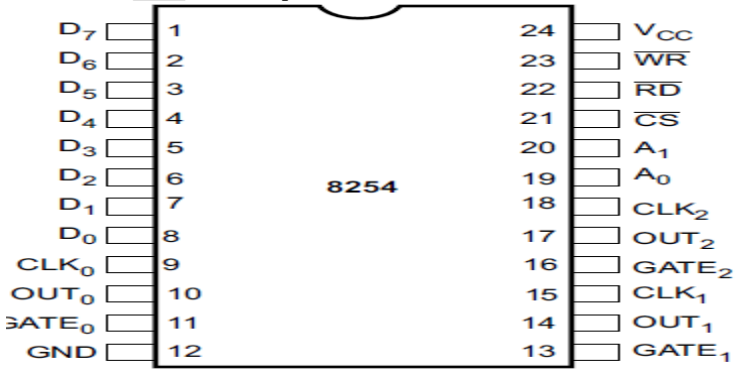
2) where as 8253 can operate upto 2.6 MHz

Three counters are identical presettable, and can be programmed for either

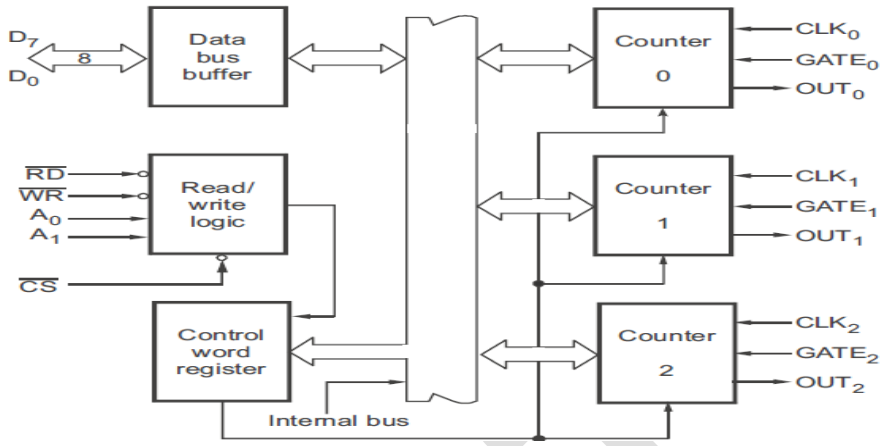
binary or BCD count.

4) Counter can be programmed in six different modes.

5) Compatible with all Intel and most other microprocessors



Block Diagram



Data Bus Buffer :
This tri-state, bi-directional, 8-bit buffer is used to interface the 8253/54 to the system data bus. The Data bus buffer has three basic functions.
1. Programming the modes of 8253/54.
2. Loading the count registers.
3. Reading the count values.

Read/Write Logic: The Read/Write logic has five signals : RD, WR, CS and the address lines A0 and A1. In the peripheral I/O mode, the RD, and WR signals are connected to IOR and IOW, respectively.

Control Word Register: This register is accessed when lines A0 and A1 are at logic 1. It is used to write a command word which specifies the counter to be used (binary or BCD), its mode, and either a read or write operation.

Counters: These three functional blocks are identical in operation. Each counter consists of a single, 16 bit, pre-settable, down counter.

Operational Description

Programming the 8253/54 : Each counter of the 8253/54 is individually programmed by writing a control word into the control word register (A0 - A1 = 11).

WRITE Operation :
1. Write a control word into control register.
2. Load the low-order byte of a count in the counter register.
3. Load the high-order byte of count in the counter register.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC_1	SC_0	RW_1	RW_0	M_2	M_1	M_0	BCD

SC - Select counter

SC_1	SC_0	
0	0	Select counter 0
0	1	Select counter 1
1	0	Select counter 2
1	1	Illegal for 8253 Read -Back command for 8254 (See Read operations)

M - Mode

M_2	M_1	M_0	
0	0	0	Mode 0
0	0	1	Mode 1
x	1	0	Mode 2
x	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

RW - Read /Write

RW_1	RW_0	
0	0	Counter latch command (See Read operations)
0	1	Read / Write least significant byte only
1	0	Read / Write most significant byte only
1	1	Read / write least significant byte first, then most significant byte

BCD :

0	Binary counter 16 - bits
1	Binary coded decimal (BCD) Counter (4 Decades)

Note : Don't care bits (x) should be 0 to ensure compatibility with future Intel products

10. Explain terms synchronous, baud rate, parity, half and full duplex transmission.

11. Explain the block diagram and the functions of each block of the 8251 USART (Programmable Communication Interface).

The 8251A is the industry standard Universal Synchronous/Asynchronous Receiver/Transmitter (USART) designed for data communications with microprocessor families such as MCS-48, 80, 85, and iAPX 86, 88. The 8251A is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM "bi-sync"). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission

block diagram

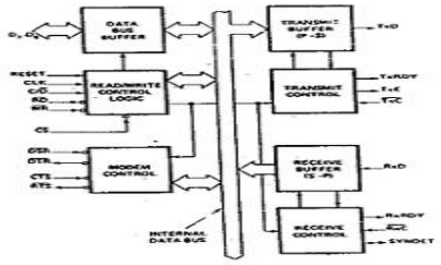
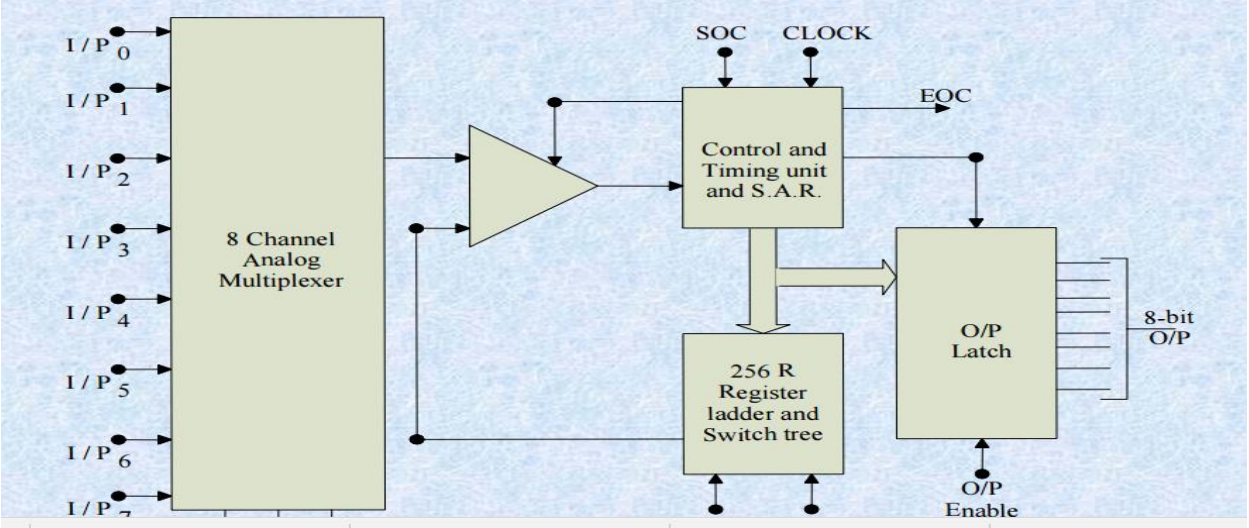


Figure 1. Block Diagram

11. Explain the procedure of interfacing D/A and A/D converter circuit.

In most of the cases, the PIO 8255 is used for interfacing the analog to digital converters with microprocessor. • We have already studied 8255 interfacing with 8086 as an I/O port, in previous section. This section we will only emphasize the interfacing techniques of analog to digital converters with 8255.



• I/P 0 –I/P 7 Analog inputs
• ADD A,B,C Address lines for selecting analog inputs.
• O 7 – O 0 Digital 8-bit output with O 7 MSB and O 0 LSB
• SOC Start of conversion signal pin
• EOC End of conversion signal pin
• OE Output latch enable pin, if high enables output
• CLK Clock input for ADC I

12. Illustrate traffic light controller with its interfacing procedure and programming

Traffic light controller interface module is designed to simulate the function of four way traffic light controller. Combinations of red, amber and green LED's are provided to indicate Halt, Wait and Go signals for vehicles.

Combination of red and green LED's are provided for pedestrian crossing. 36 LED's are arranged in the form of an intersection. A typical junction is represented on the PCB with comprehensive legend printing.

At the left corner of each road, a group of five LED's (red, amber and 3 green) are arranged in the form of a T-section to control the traffic of that road. Each road is named North (N), South(S), East (E) and West (W). LED's L1, L10, L19 & L28 (Red) are for the stop signal for the vehicles on the road N, S, W, & E respectively. L2, L11, L20 & L29 (Amber) indicates wait state for vehicles on the road N, S, W, & E respectively. L3, L4 & L5 (Green) are for left, strait and right turn for the vehicles on road S. similarly L12-L13-L14, L23-L22-L21 & L32-L31-L30 simulates same function for the roads E, N, W respectively. A total of 16 LED's (2 Red & 2 Green at each road) are provided for pedestrian crossing.

L7-L9.L16-L18, L25-L27 & L34-L36 (Green) when on allows pedestrians to cross and L6-L8, L15-L17, L24-L26 & L33-L35 (Red) when on alarms the pedestrians to wait.

To minimize the hardware pedestrian's indicator LED's (both red and green are connected to same port lines (PC4 to PC7) with red inverted.

Red LED's L10 & L28 are connected to port lines PC2 & PC3 while L1 & L19 are connected to lines PC0 & PC1 after inversion. All other LED's (amber and green) are connected to port A & B.

MEMORY ADDRESS	OPCODE	MNEUMONICS	COMMENTS

		START:
		MOV AX,@DATA
		MOV DS,AX
		MOV AL,80H
		MOV DX,CWR
		OUT DX,AL	

```
MOV AL,F3H
MOV DX,PORTC
OUT DX,AL
MOV AL,FFH
MOV DX,PORTA
OUT DX,AL
MOV AL,FFH
MOV DX,PORTB
OUT DX,AL
MOV CL,03H
CALL DELAY
TOP:
MOV AL,EEH
MOV DX,PORTA
OUT DX,AL
MOV AL,EEH
MOV DX,PORTB
OUT DX,AL
MOV CL,02H
CALL DELAY

MOV AL,FCH
MOV DX,PORTC
OUT DX,AL
MOV AL,7DH
MOV DX,PORTA
OUT DX,AL
MOV AL,57H
MOV DX,PORTB
OUT DX,AL
MOV CL,15H
CALL DELAY

MOV AL,E7H
MOV DX,PORTB
OUT DX,AL
MOV AL,FDH
MOV DX,PORTA
OUT DX,AL
MOV AL,EDH
MOV DX,PORTA
OUT DX,AL
MOV CL,02H
CALL DELAY

MOV AL,F7H
MOV DX,PORTB
OUT DX,AL
MOV AL,F0H
MOV DX,PORTC
OUT DX,AL
MOV AL,F1H
MOV DX,PORTA
OUT DX,AL
MOV CL,15H
CALL DELAY
```

```
MOV AL,FBH
MOV DX,PORTA
OUT DX,AL
MOV AL,FBH
MOV DX,PORTB
OUT DX,AL
MOV AL,50H
MOV DX,PORTC
OUT DX,AL
MOV CL,15H
CALL DELAY

MOV AL,FEH
MOV DX,PORTA
OUT DX,AL
MOV AL,FEH
MOV DX,PORTB
OUT DX,AL
MOV CL,03H
CALL DELAY

MOV AL,FFH
MOV DX,PORTA
OUT DX,AL
MOV AL,AFH
MOV DX,PORTC
OUT DX,AL
MOV AL,EEH
MOV DX,PORTA
OUT DX,AL
MOV AL,EEH
MOV DX,PORTB
OUT DX,AL
MOV CL,02H
CALL DELAY

MOV AL,BFH
MOV DX,PORTA
OUT DX,AL
MOV AL,BFH
MOV DX,PORTB
OUT DX,AL
MOV CL,15H
CALL DELAY
JMP TOP

DELAY:
MOV BX,10H
D1:
MOV CX,0FFFFH
D2:
LOOP D2
DEC BX
JNZ D1
INT 03H
```

		END START	

.