SRI VIDYA COLLEGE OF ENGINEERING & TECHNOLOGY, VIRUDHUNAGAR

Department of Computer Science and Engineering

UNIT-III

PROCESSOR AND CONTROL UNIT

PART A

1. **Define MIPS .**

MIPS:One alternative to time as the metric is MIPS(Million Instruction Per Second) MIPS=Instruction count/(Execution time x1000000).

This MIPS measurement is also called Native MIPS todistinguish it from some alternative definitions of MIPS.

2. **Define MIPS Rate:**

The rate at which the instructions are executed at a given time.

3. **Define pipelining.**

Pipelining is a technique of decomposing a sequential process into sub operations with each sub process being executed in a special dedicated segment that operates concurrently with all other segments.

4. **Define parallel processing.**

Parallel processing is a term used to denote a large class of techniques that are used to provide simultaneous data-processing tasks for the purpose of increasing the computational speed of a computer system. Instead of processing each instruction sequentially as in a conventional computer, a parallel processing system is able to perform concurrent data processing to achieve faster execution time.

5. **Define instruction pipeline.**

The transfer of instructions through various stages of the CPU instruction cycle.,including fetch opcode, decode opcode, compute operand addresses. Fetch operands, execute Instructions and store results. This amounts to realizing most (or) all of the CPU in the form of multifunction pipeline called an instruction pipelining.

6. What are the steps required for a pipelinened processor to process the instruction?

- F Fetch: read the instruction from the memory
- D Decode: decode the instruction and fetch the source operand(s).
- E Execute: perform the operation specified by the instruction.
- W Write: store the result in the destination location

7. What are Hazards?

A hazard is also called as hurdle .The situation that prevents the next instruction in the instruction stream from executing during its designated Clock cycle. Stall is introduced by hazard. (Ideal stage)

8. State different types of hazards that can occur in pipeline.

The types of hazards that can occur in the pipelining were,

1. Data hazards.
2. Instruction hazards.
3. Structural hazards.

9. Define Data hazards

A data hazard is any condition in which either the source or the destination operands of an instruction are not available at the time expected in pipeline. As a result some operation has to be delayed, and the pipeline stalls.

10. Define Instruction hazards

The pipeline may be stalled because of a delay in the availability of an instruction. For example, this may be a result of miss in cache, requiring the instruction to be fetched from the main memory. Such hazards are called as Instruction hazards or Control hazards.

11.Define Structural hazards?

The structural hazards is the situation when two instructions require the use of a given hardware resource at the same time. The most common case in which this hazard may arise is access to memory.

12. What are the classification of data hazards?

Classification of data hazard: A pair of instructions can produce data hazard by referring reading or writing the same memory location. Assume that i is executed before J. So, the hazards can be classified as,

1. RAW hazard
2. WAW hazard

3. WAR hazard

13.Define RAW hazard : (read after write)

Instruction ‘j’ tries to read a source operand before instruction ‘i’ writes it.

14. Define WAW hazard :(write after write)

Instruction ‘j’ tries to write a source operand before instruction ‘i’ writes it.

15.Define WAR hazard :(write after read)

Instruction ‘j’ tries to write a source operand before instruction ‘i’ reads it.

16. How data hazard can be prevented in pipelining?

Data hazards in the instruction pipelining can prevented by the following techniques.

a)Operand Forwarding

b)Software Approach

17.How Compiler is used in Pipelining?

A compiler translates a high level language program into a sequence of machine instructions. To reduce N, we need to have suitable machine instruction set and a compiler that makes good use of it. An optimizing compiler takes advantages of various features of the target processor to reduce the product N*S, which is the total number of clock cycles needed to execute a program. The number of cycles is dependent not only on the choice of instruction, but also on the order in which they appear in the program. The compiler may rearrange program instruction to achieve better performance of course, such changes must not affect of the result of the computation.

18. How addressing modes affect the instruction pipelining?

Degradation of performance is an instruction pipeline may be due to address dependency where operand address cannot be calculated without available informatition needed by addressing mode for e.g. An instructions with register indirect mode cannot proceed to fetch the operand if the previous instructions is loading the address into the register. Hence operand access is delayed degrading the performance of pipeline.

19. What is locality of reference?

Many instruction in localized area of the program are executed repeatedly during some time period and the remainder of the program is accessed relatively infrequently .this is referred as locality of reference.

20. What is the need for reduced instruction chip?

- Relatively few instruction types and addressing modes.
- Fixed and easily decoded instruction formats.
- Fast single-cycle instruction execution.
- Hardwired rather than micro programmed control

21. Define memory access time?

The time that elapses between the initiation of an operation and completion of that operation ,for example ,the time between the READ and the MFC signals .This is Referred to as memory access time.

22. Define memory cycle time.

The minimum time delay required between the initiations of two successive memory operations, for example, the time between two successive READ operations.

23.Define Static Memories.

Memories that consist of circuits capable of retaining the state as long as power is applied are known as static memories.

24. List out Various branching technique used in micro program control unit?

a) Bit-Oring

b) Using Conditional Variable

c) Wide Branch Addressing

25. How the interrupt is handled during exception?

* CPU identifies source of interrupt

* CPU obtains memory address of interrupt handles

* pc and other CPU status information are saved

* Pc is loaded with address of interrupt handler and handling program to handle it.

26. List out the methods used to improve system performance.

The methods used to improve system performance are

1. Processor clock

2.Basic Performance Equation

3.Pipelining

4.Clock rate

5.Instruction set

6.Compiler

27. What are the ways to build a datapath

28. What are the control schemes available in processors

PART B

1. State and explain the different types of hazards that can occur in a pipeline.

2.Draw and explain the structure of a superscalar processor. Also explain the flow of instruction execution in it.

3. Explain the control implemation scheme in detail

4. Implement basic structure of MIPS

5. Define datahazard and instruction hazard and explain in detail

6. Explain pipelined data path and control path

7. What are the two aspects of machine instruction? Explain it .

8. .Draw and explain the modified three-bus structure of the processor suitable for four -stage pipelined execution. How this structure is suitable to provide four-stage pipelined execution?