| | SRI VIDYA COLLEGE OF ENGINEERING & TECHNOLOGY<br>COURSE PLAN | Doc.Ref:SVCSE02<br>Revision: 01<br>Date: 25/06/2018 |
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## DEPARTMENT OF COMPUTER SCIENCE ENGINEERING

ACADEMIC YEAR: 2018-2019(ODD)

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|---|---|---|---|---|---|
| Subject Code | CS8351 | L | P | T | C |
| Subject Title | DIGITAL PRINCIPLES AND SYSTEM DESIGN | 4 | 0 | 0 | 4 |
| Year / Dept / Sem | II/CSE/III | Regulation Year | 2017 | | |
| Faculty Name / Desg / Dept | Mrs.T.UTHRADEVI /AP/ECE | | | | |
| Course Prerequisite | Fundamental concepts of Logic gates and digital circuits | | | | |
| Course Objectives (CO) | CO1: To design digital circuits using simplified Boolean functions<br>CO2: To analyze and design combinational circuits<br>CO3: To analyze and design synchronous and asynchronous sequential circuits<br>CO4: To understand Programmable Logic Devices<br>CO5: To write HDL code for combinational and sequential circuits | | | | |

**CS8351 DIGITAL PRINCIPLES AND SYSTEM DESIGN** **L T P C**
**4 0 0 4**

**UNIT I BOOLEAN ALGEBRA AND LOGIC GATES** **12**

Number Systems – Arithmetic Operations – Binary Codes – Boolean Algebra and logic gates- Theorems and Properties of Boolean Algebra – Boolean functions – Canonical and Standard Forms – Simplifications of Boolean Functions using Karnaugh Map – Logic Gates – NAND and NOR Implementations.

**UNIT II COMBINATIONAL LOGIC** **12**

Combinational Circuits – Analysis and Design Procedures – Binary Adder – Subtractor – Decimal Adder – Binary Multiplier – Magnitude Comparator- Decoders – Encoders – Multiplexer – Introduction yo HDL – HDL Models of Combinational circuits.

**UNIT III SYNCHORONOUS SEQUENTIAL LOGIC** **12**

Sequential circuits – Storage Elements – Latches – Flip-flops – Analysis of Clocked Sequential Circuits – State Reduction and Assignment – Design Procedure – Registers – Counters – HDL Models of Sequential Circuits.

**UNIT IV ASYNCHORONOUS SEQUENTIAL LOGIC** **12**

Analysis and Design of Asynchronous Sequential Circuits – Reduction of State and Flow Tables – Race – free state assignment – Hazards.

**UNIT V MEMORY AND PROGRAMMABLE LOGIC** **12**

RAM – Memory Decoding – Error Detection and Correction – ROM – Programmable Logic Array - Programmable Array Logic – Sequential Programmable Devices

**TOTAL: 60 Periods**

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| Related Website URLs | W1: wps.pearsoned.co.uk/wps/media/objects/1244/.../Chap09.ppt<br>W2: www.colorado.edu/physics/...sp12/.../Exp_9_Spring12_re.pdf<br>W3:www.cl.cam.ac.uk/teaching/0708/.../Digital_Electronics_pdf.pdf<br>W4:www.ni.com/digital logic<br>W5:www.asic-world.com/digital/tutorial |
| Related Video Course Materials (min. 4 no.s) | V1: www.youtube.com/watch?v=CeD2L6KbtVM<br>V2: nptel.ac.in/courses/117106086/<br>V3: nptel.ac.in/video.php?subjectId=117106086<br>V4: www.electrodictien.com/digital-electronics<br>V5: www.youtube.com/watch?v=Kedfk89gt34 |

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| Expected Course Outcome (ECO) | At the end of the course, the students should be able to:<br>ECO1:Simplify Boolean functions using K-Map.<br>ECO2: Design and Analyze Combinational and Sequential Circuits.<br>ECO3: Implement designs using Programmable Logic Devices .<br>ECO4: Write HDL codes for Combinational and Sequential circuits. |
| **Bridging the Curriculum Gap** (Additional Topics beyond syllabus / Seminars / Assignments) | BCG1: Introduction to VHDL<br>BCG2: Fast adders-Carry select adder<br>BCG3: ROM, RAM<br>BCG4: Analysis & Synthesis of Logic functions using Decoders(Virtual Lab)<br>BCG5: Analysis & Synthesis of Basic Flip Flops(Virtual Lab) |
| Text books | **T1: M. Morris R. Mano, Michael D. Ciletti, "Digital Design: With an Introduction to the Verilog HDL, VHDL, and SystemVerilog", 6th Edition, Pearson Education, 2017.** |
| Reference Books | **R1**: G. K. Kharate, Digital Electronics, Oxford University Press, 2010.<br>**R2**: John F. Wakerly, Digital Design Principles and Practices, Fifth Edition, Pearson Education, 2017.<br>**R3**: Charles H.Roth. "Fundamentals of Logic Design", 6th Edition, Thomson Learning, 2013.<br>**R4**: Donald D.Givone, "Digital Principles and Design", TMH, 2003.<br>**R5**: S. Salivahanan and S. Arivazhagan, "Digital Circuits and Design", 3rd Edition., Vikas Publishing House Pvt. Ltd, New Delhi, 2006.<br>**R6**: Sanjay Kumar Suman, L.Bhagyalakshmi, S.Porselvi "Digital Principles and System Design", Vijay Nicole Edition. |

**Mapping of CO & PO(Specify the PO's)**

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CO1 | C,1 | | | | | | D,1 | | | | | |
| CO2 | | E,2 | | | | | | | | | | |
| CO3 | | | D,1 | | C,1 | | | F,2 | | | | |
| CO4 | | | | | | | | | | | | |
| CO5 | C,9 | | | | | | | | | | | |
| CO6 | | | | | | F,2 | | | | | | |

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| S.No | Topic Name | Book | Page no | Mode of delivery | No of hrs | Cumu-lative hrs |
|---|---|---|---|---|---|---|
| | **UNIT I BOOLEAN ALGEBRA AND LOGIC GATES** | | | | | |
| 1 | Number Systems | R5 | 01 | BB | 1 | 1 |
| 2 | Arithmetic Operations – Binary Codes | R5 | 11 | BB | 1 | 2 |
| 3 | Boolean Algebra and logic gates- | R5 | 43 | BB | 1 | 3 |
| 4 | Theorems and Properties of Boolean Algebra – Boolean functions | R5 | 48 | BB | 2 | 5 |
| 5 | Canonical and Standard Forms | R5 | 55 | BB | 2 | 7 |
| 6 | Simplifications of Boolean Functions using Karnaugh Map | R5 | 62 | BB | 2 | 9 |
| 7 | Logic Gates | R5 | 84 | BB | 1 | 10 |
| 8 | NAND and NOR Implementations | - | Notes | BB | 2 | 12 |
| 9 | Tutorial | - | - | BB | 2 | 14 |
| | **UNIT – II COMBINATIONAL LOGIC** | | | | | |
| 10 | Combinational Circuits | R5 | 173 | BB | 1 | 15 |
| 11 | Analysis and Design Procedures | R5 | 173 | BB | 1 | 16 |
| 12 | Binary Adder, Subtractor, Decimal Adder | R5 | 174 | BB | 2 | 18 |
| 13 | Binary multiplier, binary divider | R5 | 193 | BB | 1 | 19 |
| 14 | Multiplexer | R5 | 199 | BB | 1 | 20 |
| 15 | Demultiplexer | R5 | 211 | BB | 1 | 21 |
| 16 | Decoder | R5 | 217 | BB | 1 | 22 |
| 17 | Encoder | R5 | 232 | BB | 1 | 23 |
| 18 | Magnitude comparator | R5 | 254 | BB | 1 | 24 |
| 19 | Introduction to HDL – HDL Models of Combinational circuits | R5 | 641 | BB | 2 | 26 |
| 20 | Tutorial | - | - | BB | 2 | 28 |
| | **UNIT – III SYNCHORONOUS SEQUENTIAL LOGIC** | | | | | |
| 21 | Sequential circuits – Storage Elements | R5 | 469 | BB | 1 | 29 |
| 22 | Latches | R5 | 267 | BB | 1 | 30 |
| 23 | Flip-flops.(T, D, JK, SR, MS) | R5 | 272 | OHP | 3 | 33 |
| 24 | Analysis of Clocked Sequential Circuits | R5 | 506 | BB | 1 | 34 |
| 25 | State Reduction and Assignment, Design Procedure | R5 | 472 | BB | 2 | 36 |
| 26 | Registers (SISO,PIPO,SIPO,PISO) | R5 | 357 | OHP | 1 | 37 |
| 27 | Counters (Sync,async) | R5 | 373 | BB | 3 | 40 |
| 28 | HDL Models of Sequential Circuits | R5 | 665 | BB | 2 | 42 |
| 29 | Tutorial | - | - | BB | 2 | 44 |

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| | **UNIT – IV ASYNCHORONOUS SEQUENTIAL LOGIC** | | | | | |
| 30 | Analysis and Design of Asynchronous Sequential Circuits – | R5 | 527 | BB | 2 | 46 |
| 31 | Reduction of State and Flow Tables | R5 | - | Notes | 2 | 48 |
| 32 | Race | R5 | 544 | BB | 1 | 49 |
| 33 | Free state assignment | R5 | 547 | BB | 1 | 50 |
| 34 | Hazards. | R5 | 545 | BB | 2 | 52 |
| 35 | Tutorial | - | - | BB | 2 | 54 |
| | **UNIT – V MEMORY AND PROGRAMMABLE LOGIC** | | | | | |
| 36 | RAM | R5 | 422 | BB | 1 | 55 |
| 37 | Memory Decoding | R5 | 435 | BB | 1 | 56 |
| 38 | Error Detection and Correction | R5 | - | Notes | 2 | 58 |
| 39 | ROM | R5 | 400 | BB | 2 | 60 |
| 40 | Programmable Logic Array | R5 | 444 | OHP | 2 | 62 |
| 41 | Programmable Array Logic | R5 | 452 | BB | 2 | 64 |
| 42 | Sequential Programmable Devices | R5 | - | Notes | 2 | 66 |
| 43 | Tutorial | - | - | BB | 2 | 68 |

| | ***Prepared by*** | ***Approved by*** |
|---|---|---|
| Signature | G.U | P.Balaf |
| Name | G.UTHRADEVI | P.BALAGANESH |
| Designation | Assistant Professor / ECE | Professor & HOD/ECE |
| Signed date | 28.06.2018 | 28-06-2018 |

Endorsed
(R+1)